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FINITE ELEMENT MODELING AND THERMAL SIMULATIONS OF TRANSISTOR INTEGRATED CIRCUITS

William J. Bocchi

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This report documents finite element thermal simulations of the driver amplifier of a C-band transmit/receive radar module currently under life test at the Rome Air Development Center. Steady state and transient finite element thermal simulations were performed to determine the temperature distribution within the gate regions of the transistor cells of a gallium arsenide chip. Other accomplishments include identification of the proper finite element modeling procedures and techniques and investigation of correlating infrared thermal measurements with finite element analytical results.

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0.0 EXECUTIVE SUMMARY

The purpose of this effort is to determine the means to acquire knowledge about the temperatures within Microwave/Millimeter Wave Monolithic Integrated Circuits (MIMIC). One of the major technical concerns of these devices is unacceptable reliability performance due to high temperatures in regions of the integrated circuits where large heat dissipations occur. Finite element thermal simulations make possible a prediction of the temperatures due to heat dissipations in the extremely small regions of an integrated circuit (IC) and also under conditions where temperatures change very rapidly with time.

C-band transmit/receive radar modules are currently undergoing life testing at the Rome Air Development Center (RADC). Finite element thermal simulations are performed in order to determine the temperature increase between the module heat sink and the hottest regions within the transistor cells of the gallium arsenide chip used in the module driver amplifier. Several 3-dimensional and 2-dimensional finite element models are developed, and both steady state and transient simulations are performed. This work is performed at RADC using the Numerically Integrated Elements for Systems Analysis (NISA) software. Other accomplishments include identification of the proper finite element modeling procedures and techniques and investigation of correlating infrared (IR) thermal measurements with finite element analytical results. Modeling procedures and techniques include 2-dimensional vs. 3-dimensional modeling, use of symmetry and adiabatic lines of zero heat flow, thermal effects of IC metallization, and various methods of simulating heat generation.

The finite element simulations show significant heat flow in all three dimensions. If computer resources are available, 3-D simulations should be performed and 2-D analyses avoided. For practical purposes, the source and drain metallization has a minor effect in reducing temperatures and can be neglected in finite element thermal simulations. It also appears unnecessary to model heat generation with cylindrical-shaped elements. Transient simulations are essential if the device operates in a pulsed mode. For this device, it would take 6 ms for steady state conditions to be reached. Therefore, any on/off cycling less than 6 ms requires a transient thermal simulation. The steady state results for this amplifier dissipating 2.31 watts of average heat show a 90°C temperature rise above the heat sink temperature. The transient simulation shows peak values 55°C higher than steady state results with a 1 ms on/3 ms off pulse.

A procedure is proposed which would allow an averaged finite element temperature to be calculated that would be similar to the averaging done by an IR imaging system. This would make possible a comparison of finite element results with IR measured results even though the IR sensor averages the temperatures over a relatively large region compared to the heat generation region. Modifications to the finite element model material properties could be made until satisfactory agreement between the averaged finite element temperature and the measured IR temperature for the device in a nonpulsed mode of operation has been achieved. Because the IR sensor cannot follow the pulsed response of the transistor, the adjusted transient finite element simulation should be used for the best estimate of the highest temperatures within the IC.

1.0 INTRODUCTION

A broad range of advanced microwave and millimeter wave devices using monolithic analog integrated circuits is being developed for the Department of Defense. One of the major technical concerns of these devices is unacceptable reliability performance due to high temperatures in regions of the integrated circuits where large heat dissipations occur. Therefore, it is important to determine the maximum expected temperatures within these devices prior to production and testing in order to avoid operational reliability problems later on.

This report describes the procedures and the techniques to perform finite element thermal simulations of analog devices in order to predict operating temperatures. The finite element method makes it possible to simulate 3-dimensional heat transfer under both steady state and transient thermal conditions. Three 3-dimensional models will be described. This report will discuss the use of symmetry, determination of overall model dimensions, determination of minimum element size, the effect of metallization on maximum temperatures, and heat generation methods. Also, 2-dimensional versus 3-dimensional simulations will be examined. Both steady state and transient simulations will be described. Finally, the results of the finite element simulations will be used to show how the combination of finite element results and infrared measured temperatures can be correlated in order to make better assessments of maximum temperatures within the IC.

2.0 MODELING TECHNIQUES

The objective of a finite element simulation is to determine the maximum temperatures within a given device during its operation. The

fundamental problem in achieving this objective is the small feature size of the region of interest and the relatively large region that lies between the areas of heat generation and the heat sink. A single thermal network covering all heat transfer from heat source to final heat sink is not necessary even though ultimately one desires to know the temperature difference between those two regions. The technique of using a succession of finite element models along with the use of geometric and thermal symmetry to reduce finite element model size will be demonstrated for a C-band radar transmit/receive module manufactured by General Electric Co. This device is currently being life tested at the Rome Air Development Center, and knowledge of maximum device operating temperature is essential for reliability assessments. The device, with its cover removed, is shown in Figure 1 and contains two sections. The left side is the controller section, and the right side is the module section. The module section is shown in Figure 2. The first step would be to model the entire chassis and apply the thermal loads at appropriate node points in order to determine the temperature distribution along the bottom surface of the chassis. The module components are attached to an aluminum chassis which, in turn, is attached to a heat sink plate. Prior thermal analyses and measurements performed by General Electric showed that the temperatures in the chassis floor were uniform and only 5°C higher than the heat sink plate. Given this information, one can begin the modeling at the point where the component of interest is attached to the chassis floor.

One of the high-heat-producing components in the module is the driver amplifier identified in Figure 2. This component produces a peak value of 9 watts of heat. The average heat produced is 2.31 watts. The driver amp

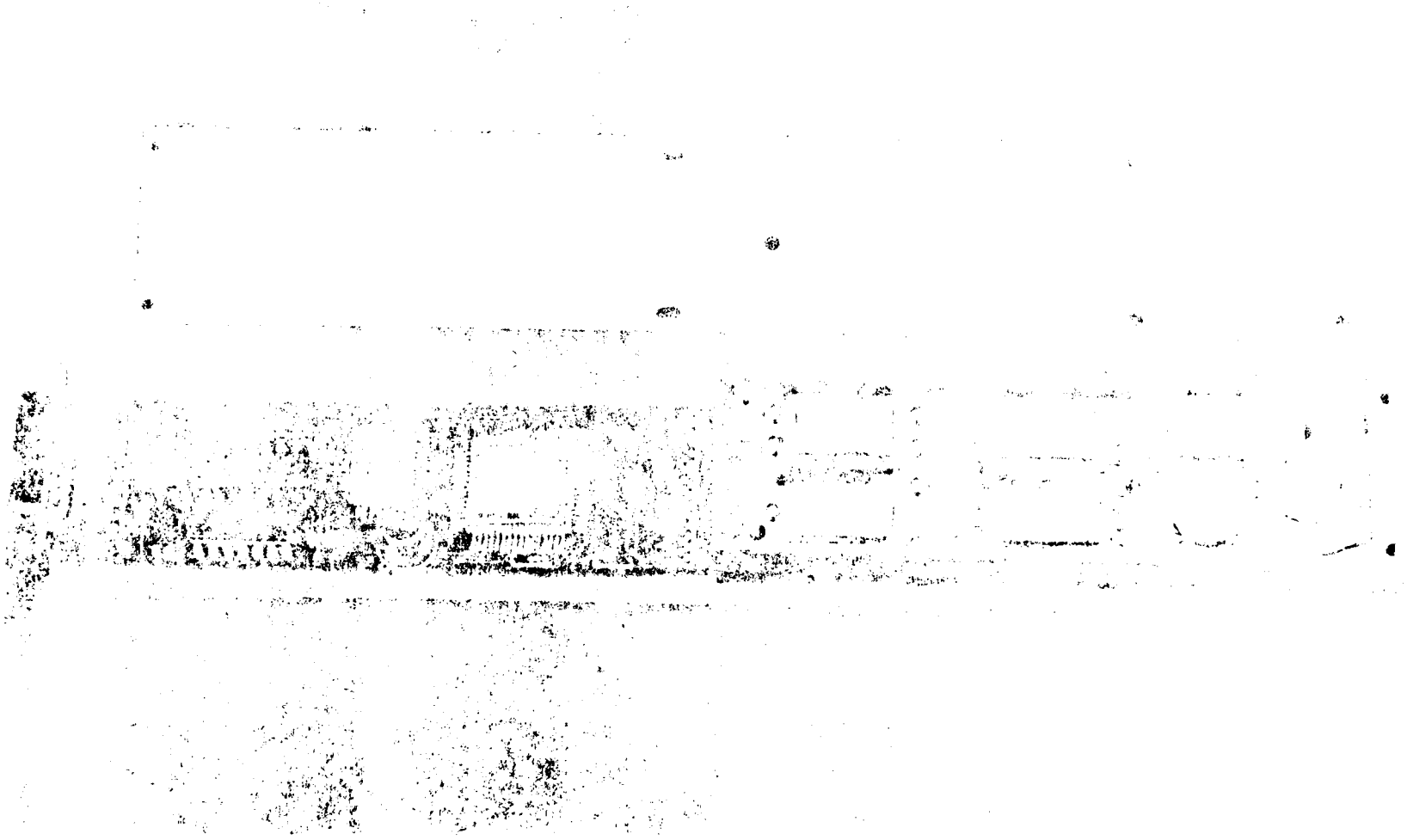


FIGURE 1: C-BAND MODULE AND CONTROLLER

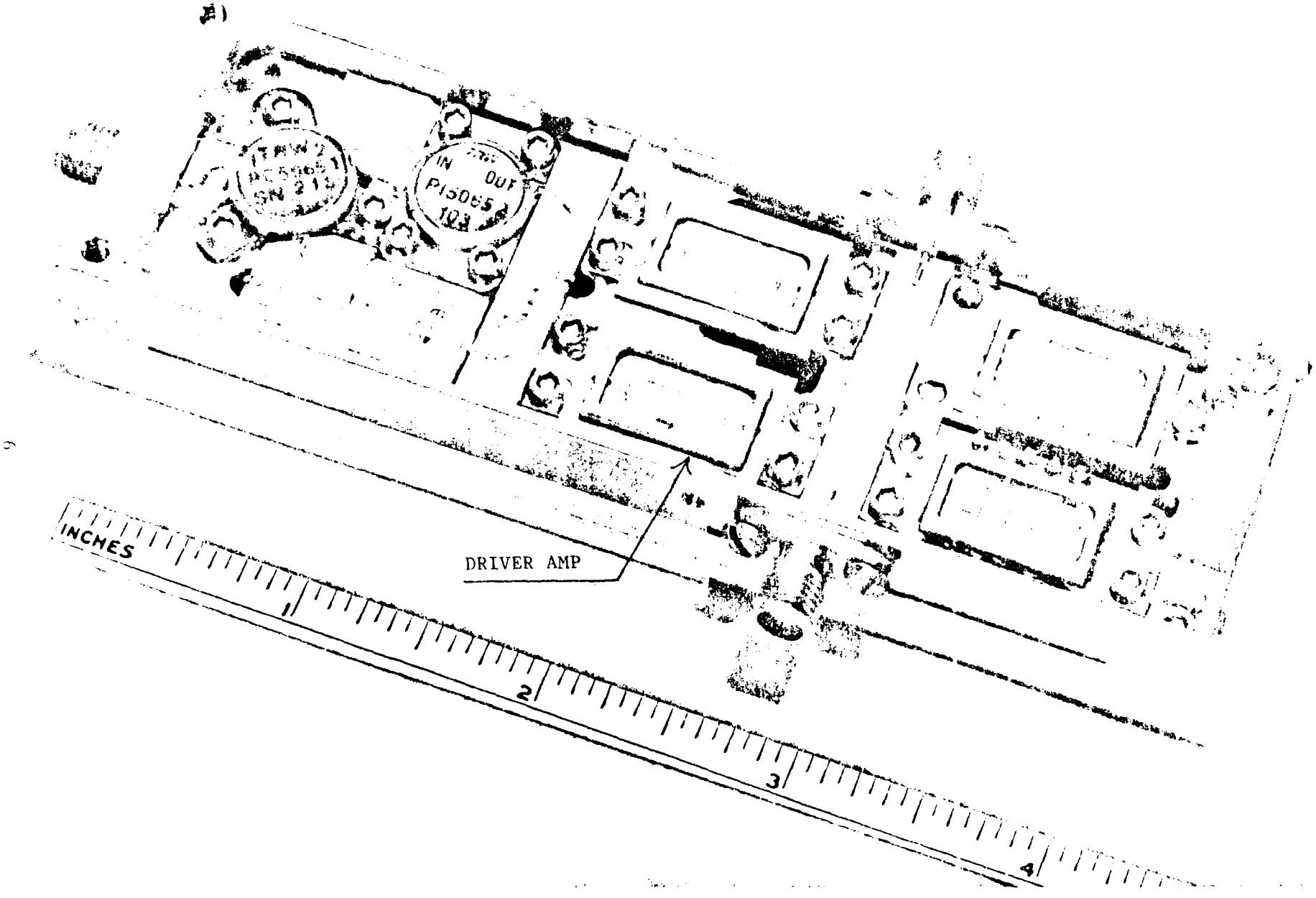


FIGURE 2: C-BAND MODULE

is shown in Figure 3. There are six transistor cells for the input and output stages (2 input, 4 output). The transistors use a gallium arsenide chip. The first issue to be addressed will be the amount of chip to be modeled.

2.1 USING SYMMETRY

Examination of Figure 3 shows a line of geometric symmetry that separates the chip into two sections, each containing one input and two output transistor cells. If an assumption of equal heat dissipation between all output stages and also equal heat dissipation between the two input stages is made, then this line of geometric symmetry is also a line of thermal symmetry in that it is an adiabatic line with no heat transfer across it. Thus, there would be equal temperatures on each side at equal distances from the line. One might also speculate that a line separating the two output stage cells is also a line of symmetry. Furthermore, one might speculate that lines that pass through one single cell - thus dividing the cell into four sections giving a model of only one-quarter of the cell - might also be lines of symmetry. If thermal analysis results show both output cells at the same maximum temperatures with a symmetrical temperature distribution on each side of the dividing line between them, then the speculation would be correct. A finite element model of one half of the chip will be used to show these thermal gradients.

2.2 CHIP 3-D MODEL

Using the known line of symmetry shown in Figure 3, three field effect transistor (FET) cells are modeled. The object of this simulation is to study the horizontal heat transfer and <u>not</u> to determine the maximum temperatures between the sources and drains of a single transistor cell. These

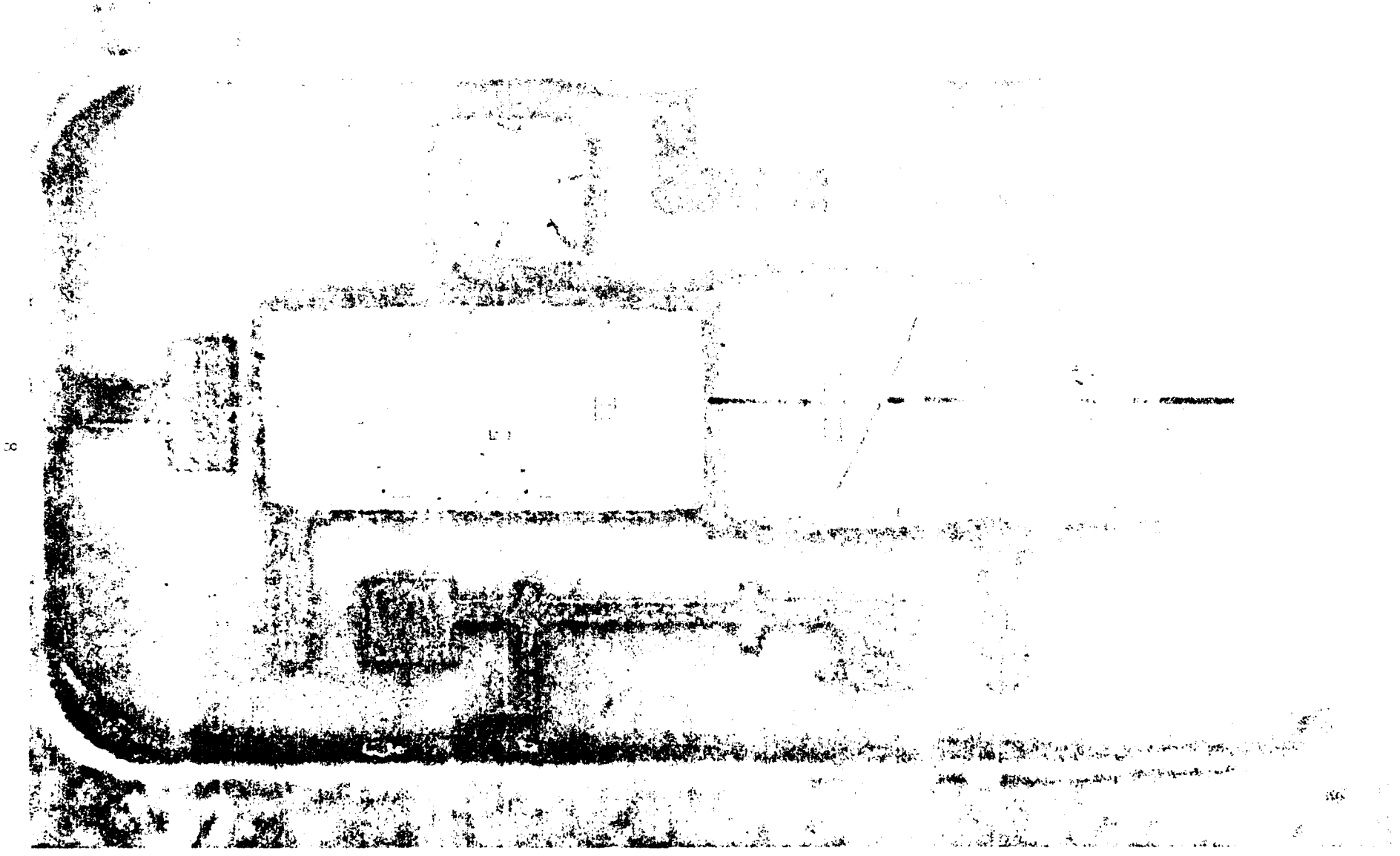


FIGURE 3: DRIVER AMP

maximum temperatures will be determined using follow on models of a small region of the chip. Therefore, only the gallium arsenide chip (.004 inches thick), a .001 inch thick layer of silver filled epoxy, a .001 inch thick layer of copper, and the beryllia substrate (.015 inches thick) will be modeled. These dimensions, as well as material properties, are from General Electric AMEA&T Report Number 87-21, "Thermal Analysis of T/R Module for ATR" by F. T. Wenthen. The entire 4 mm (.158 inches) length of the chip will be modeled. The one half chip width is 1 mm. A very important consideration in finite element analysis of microelectronic devices is the potential for error caused by numerical operations with small numbers. Therefore, all dimensions, nodal coordinates, and material properties use micrometers. Also, all temperatures are degrees centigrade. The meshed model uses elements 125 micrometers X 125 micrometers. The heat is generated as a uniform flux applied to the top surface of the appropriate elements. Each FET cell is modeled with four elements (a 250 micrometer X 250 micrometer region). The heat input is:

2.31 watts/chip X 1 chip/6 cells X 1 cell/250 X 250 square micrometers = 6.16×10^{-6} watts/square micrometer

Table 1 gives the material properties used for this and all succeeding simulations.

Figure 4 shows the steady state temperature results. An arbitrary value of 100 degrees was used for the bottom surface. Looking at the top surface of the chip in the 3-D view and studying the temperature gradients in the X-direction (chip width direction), one can see that the effect of having two cells next to each other is to create an adiabatic line along the center of the model at X = 500 micrometers (halfway across the model).

	THERMAL CONDUCTIVITY	SPECIFIC HEAT	DENSITY
	W/μM°C	Joules/Kg°C	$Kg/(\mu M)^3$
[illegible]	3.31×10^{-5}	335	5.32×10^{-15}
[illegible]	1.73×10^{-6}	2083	2.41×10^{-15}
[illegible]	3.94×10^{-4}	386	8.86×10^{-15}
[illegible]	2.12×10^{-4}	1248	3.04×10^{-15}
[illegible]	2.39×10^{-4}	203	8.86×10^{-15}
INVAR*	1.04×10^{-5}	386	8.05×10^{-15}
[illegible]**	2.96×10^{-4}	***	***

*From RADC-TR-81-382, p.280

**75% times the value for copper

***Not required for steady state analysis

TABLE 1 - MATERIAL PROPERTIES

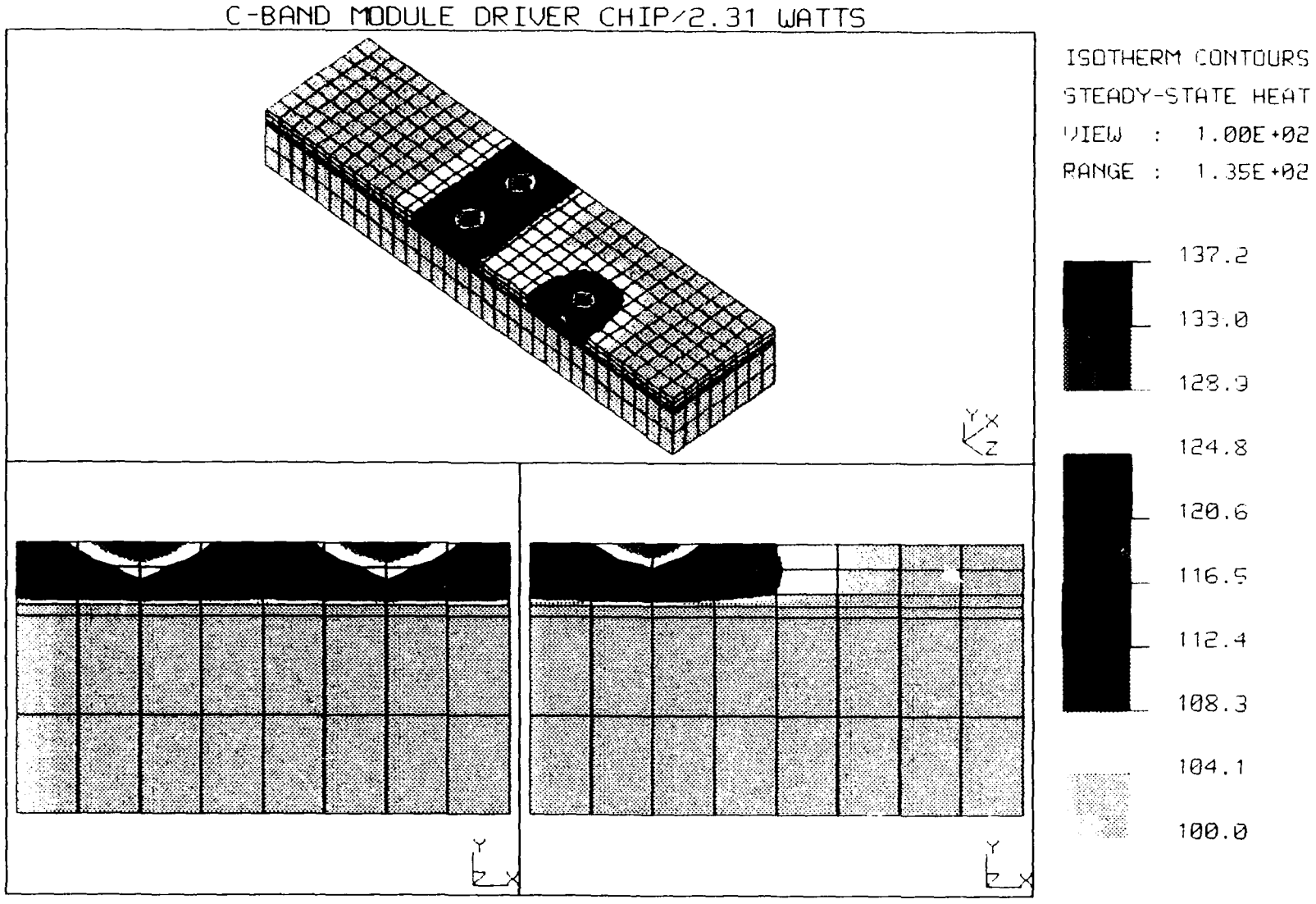


FIGURE 4: CHIP TEMPERATURES

The cross-sectional view in the X-Y plane through the center of the two cells also clearly shows the temperature symmetry on each side of the center of the model. For the single cell, however, there is no line of symmetry at the center of the model (X = 500 micrometers). Note, however, that at or beyond X = 700 micrometers, there is very little temperature gradient and one could assume an adiabatic line of zero heat transfer at this point. In addition, adiabatic lines exist at the very center of each of the two cells and for practical purposes, one could also assume an adiabatic line at the center of the single cell. Next, consider the existence of adiabatic lines along the X-direction (the transistor gate "length" direction). Looking at the top surface of the 3-D view in Figure 4, one can observe adiabatic lines through the center of each cell, midway between cells, and at or beyond Z-values where the thermal gradients disappear. Figure 5 shows all of the observed adiabatic lines. These lines determine the X and Z boundaries for follow on finite element models of smaller regions of the chip. Thus the speculations mentioned in paragraph 2.1 concerning symmetry are correct.

2.3 MODELING AND ANALYSIS OF 1/4 OF ONE FET CELL

The objectives for this model are:

1. To determine boundary conditions for a third model of an even smaller region of the chip
2. To determine adiabatic locations
3. To determine the effect of heat transfer along the source metallization.

The prior 3-D steady state simulation of three cells justifies a model that divides one cell into four sections. There are four sources, five

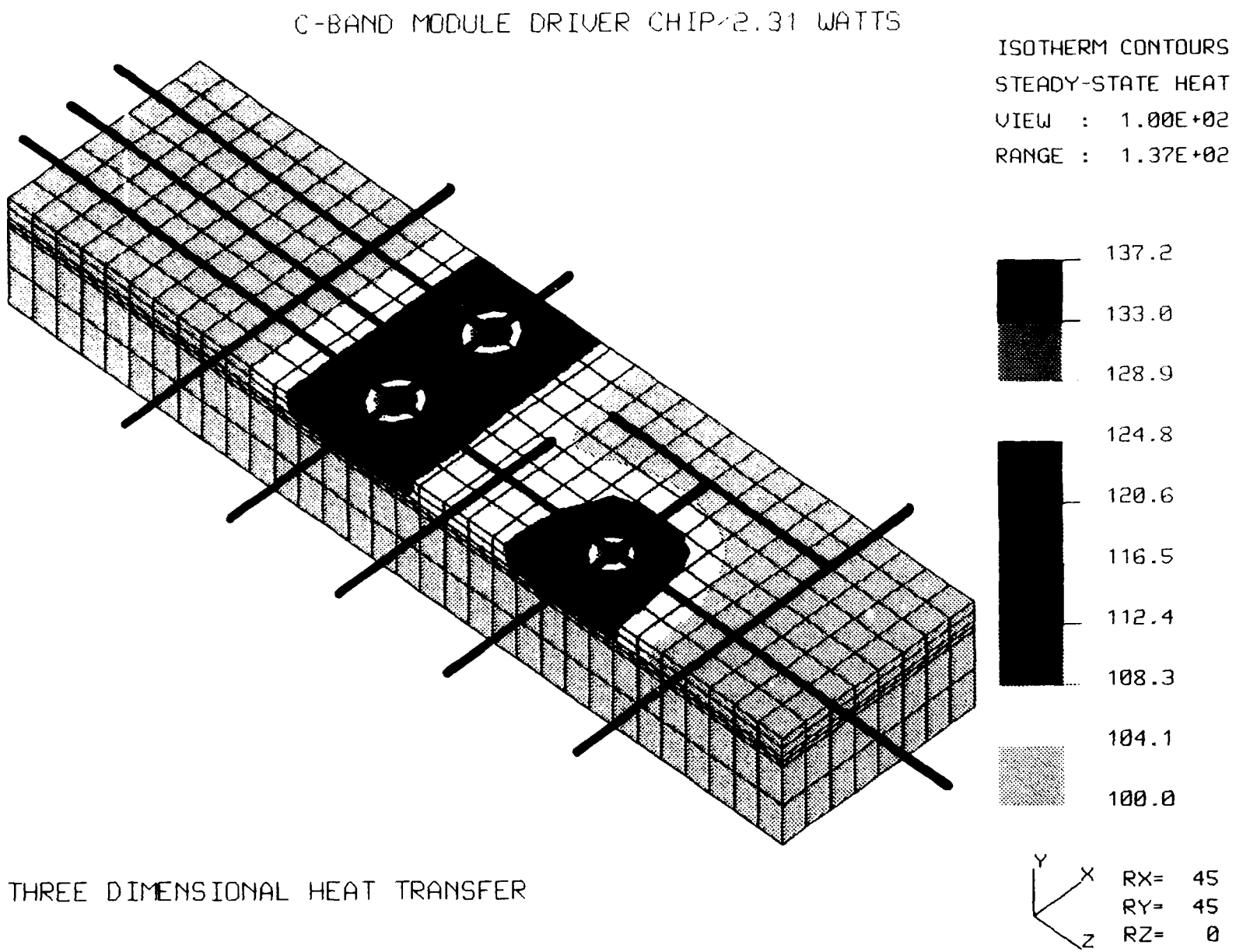


FIGURE 5: OBSERVED ADIABATIC LINES

drains, and eight gates for each cell. The center-to-center spacing between cells in the X-direction (chip width direction) is 360 micrometers. Thus the quarter model will extend from the center of a cell halfway to the center of the next cell - a dimension of 180 micrometers. The prior analysis also showed little thermal gradient beyond 500 micrometers in the Z-direction (chip length direction). Therefore, the overall dimensions of the quarter model are X = 180 micrometers and Z = 500 micrometers. The depth of the model will include all material from the chip down to the bottom of the mount. The heat in a FET cell is generated in a region represented as a half cylinder with a radius equal to the gate "length". The gate length is approximately 1 micrometer. The objectives for this model, however, can be accomplished by neglecting the space between the source and drain and by generating the heat at the node points along the lines where the source and drain elements are connected. Two sources, two and one half drains, and four gate "lines" are modeled. The gate lines are 100 micrometers "wide" in the Z-direction. Although the length of a source is 40 micrometers and the length of a drain is 30 micrometers, each was modeled to be 40 micrometers in order to use elements 20 micrometers in the X-direction. To keep aspect ratios reasonable, the model was meshed every 50 micrometers in the Z-direction. Likewise, the number of layers of elements in the Y-direction (thickness direction) was determined such that aspect ratios are less than 7.5 to 1. This resulted in a model with 1350 elements and 1760 nodes -considered to be a rather large model. Figure 6 shows the finite element model with all materials identified and the steady state results. The results show that the active region of GaAs will see a 90 degree temperature rise above the device base temperature.

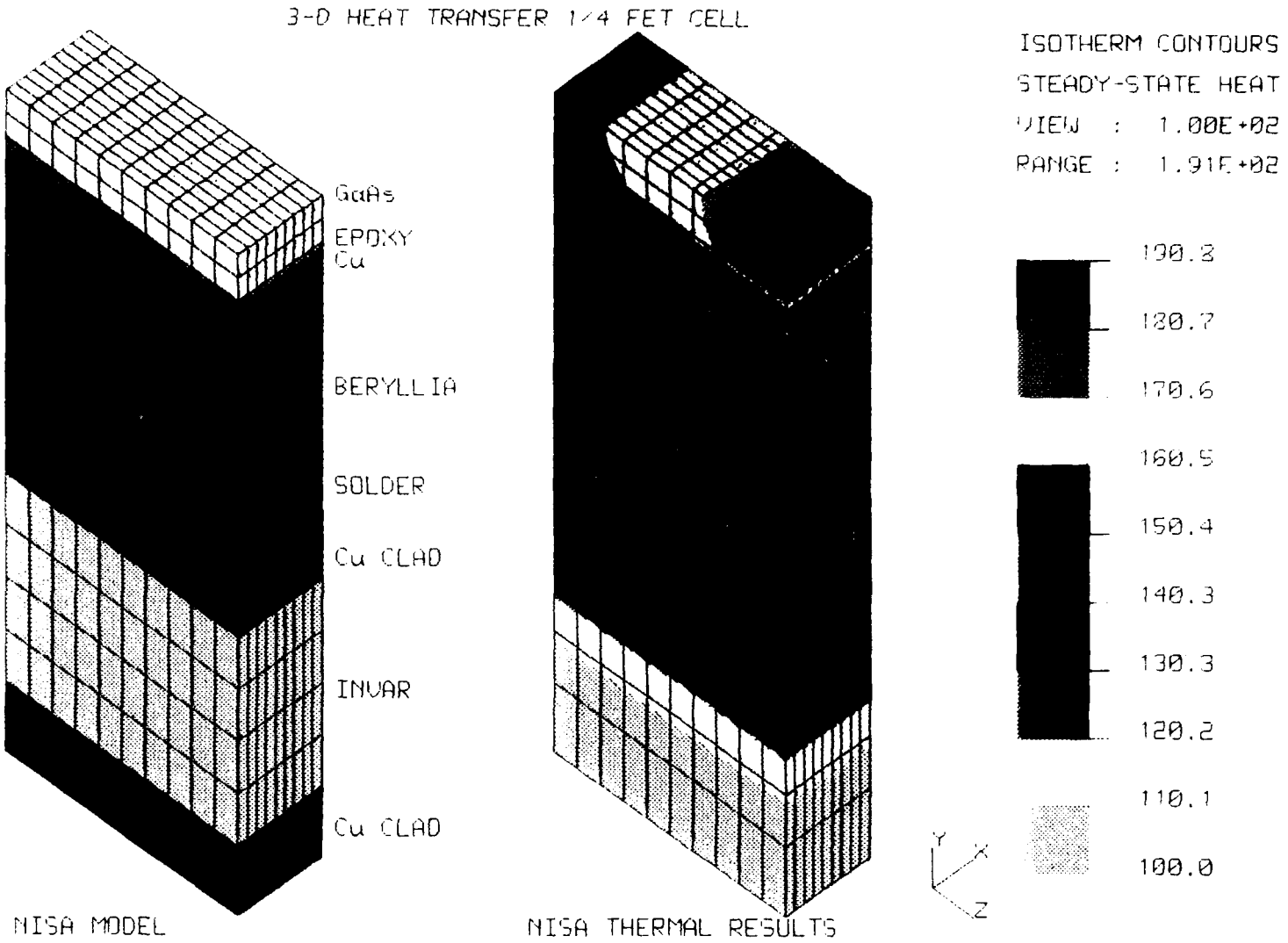


FIGURE 6: 1/4 FET CELL MODEL AND RESULTS

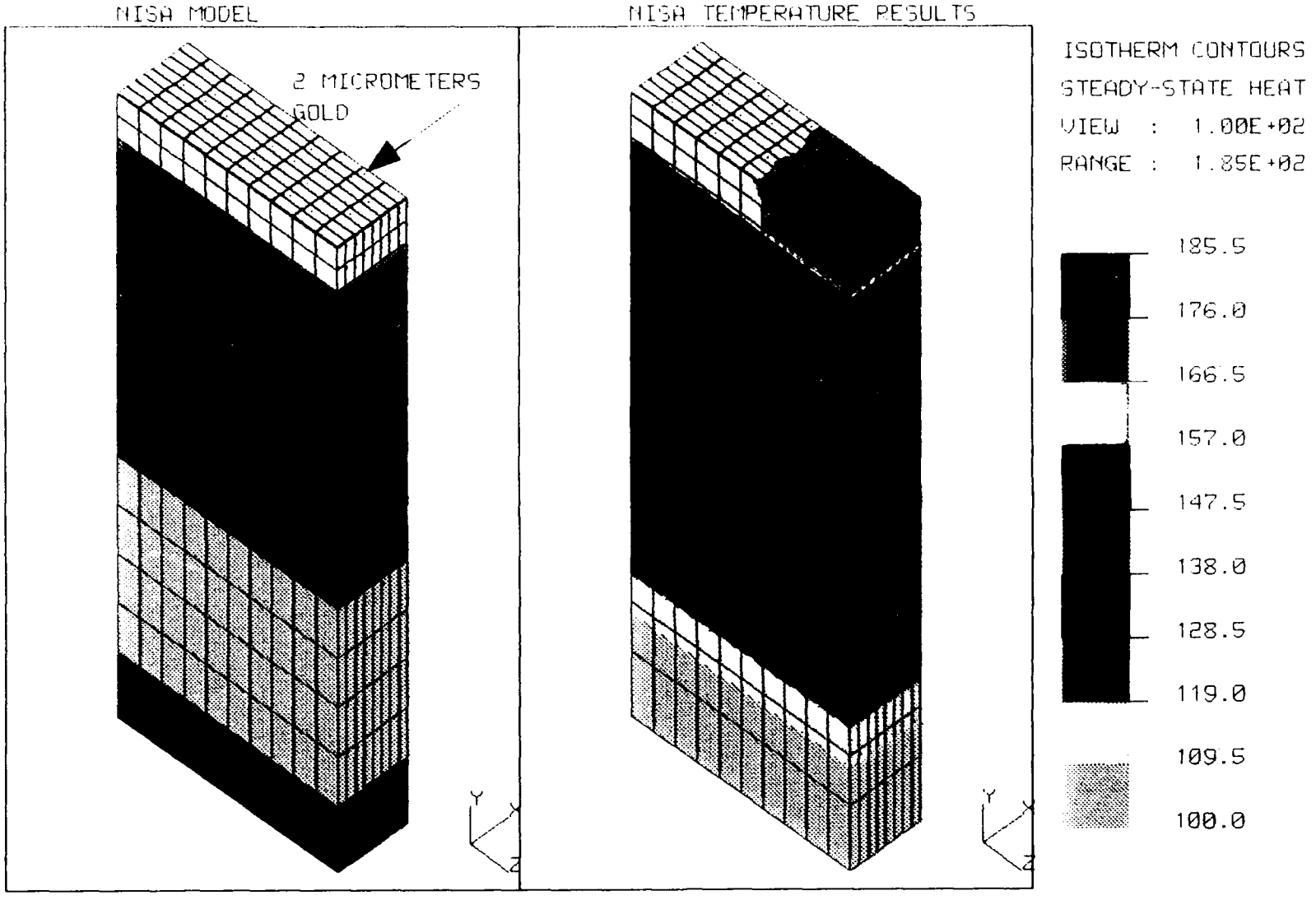
As a check, a second analysis was performed by generating heat as a flux loading over the active region of the GaAs (as was done in the chip analysis). The results were nearly identical, with a maximum temperature of 191.1 (vs. 190.8 using concentrated nodal heat generation along a line of nodes). In order to determine the effect of source and drain metallization, and having the source metal extend down through the GaAs, the model was modified by adding a 2 micrometer layer of gold. The model and results are shown in Figure 7. The maximum temperature is reduced to 185.5. Therefore, the percent reduction in chip temperature increase due to the metallization is:

$100 - (185.5 - 100)/(190.8 - 100) \times 100 = 5.84\%$ reduction in ΔT.

Because the source and drain metal in a FET are separated by a 5 micrometer space, and also the amount of metal that extends down through the via is probably less than modeled due to some of the via being filled with low conductivity epoxy or possibly being hollow, the 5.84% reduction in ΔT is most likely an upper limit. Figure 8 shows another view of the model and the temperature results for only the gold and gallium arsenide materials.

2.4 MODELING AND ANALYSIS OF A SINGLE GATE

The heat in a transistor cell is generated within the small regions between the sources and drains. Therefore, a third finite element model with small-sized elements is developed. The overall model dimensions must be reduced, and the use of symmetry and/or the application of thermal boundary conditions becomes necessary. Figure 9 shows the temperatures in the active region of the gallium arsenide material obtained from the prior one-quarter model simulation. Recall the element dimensions are 20 micrometers X 50 micrometers in the X and Z directions respectively.



3-D HEAT TRANSFER 1/4 FET CELL WITH SOURCE AND DRAIN METAL

FIGURE 7: FET CELL WITH METALLIZATION

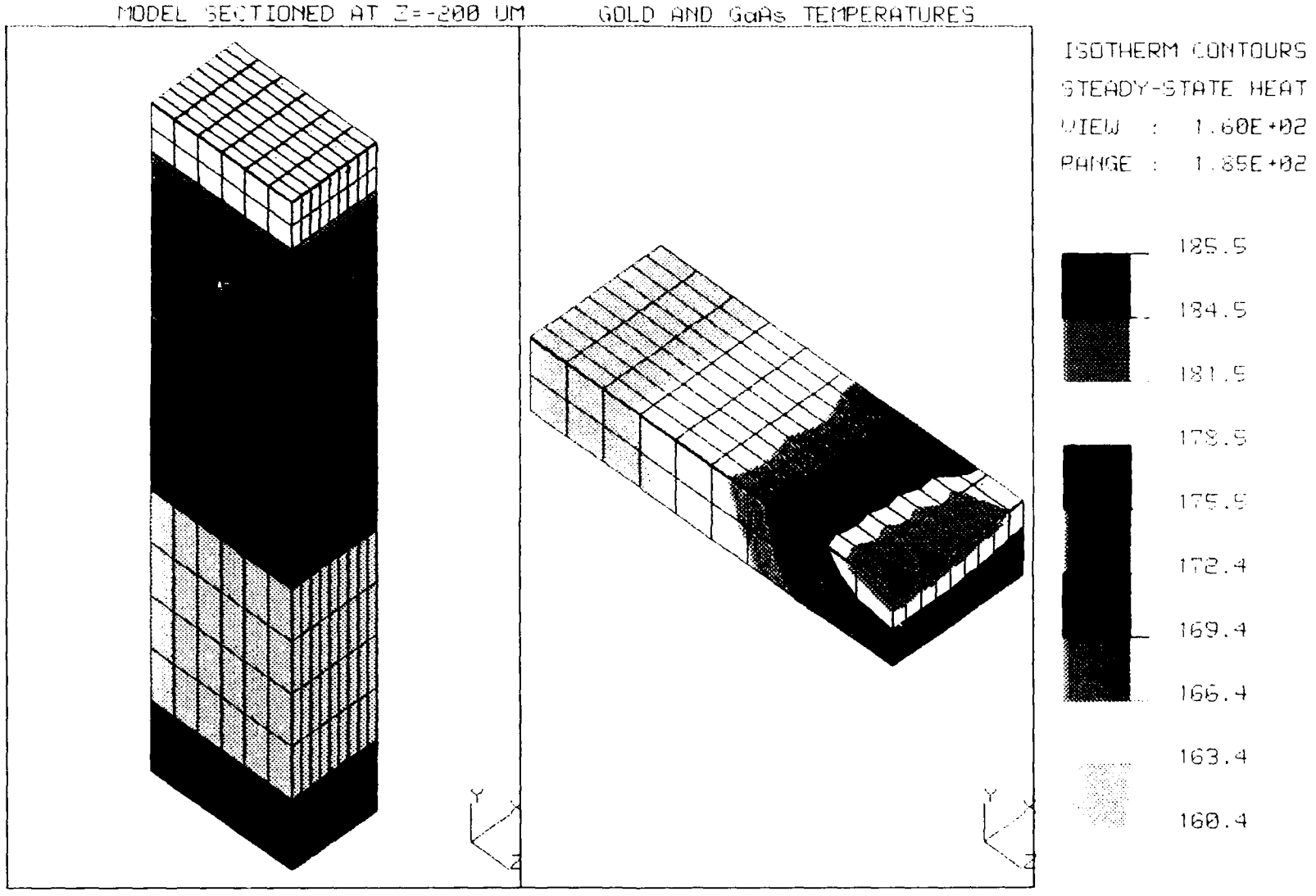


FIGURE 8: GOLD AND GALLIUM ARSENIDE TEMPERATURES

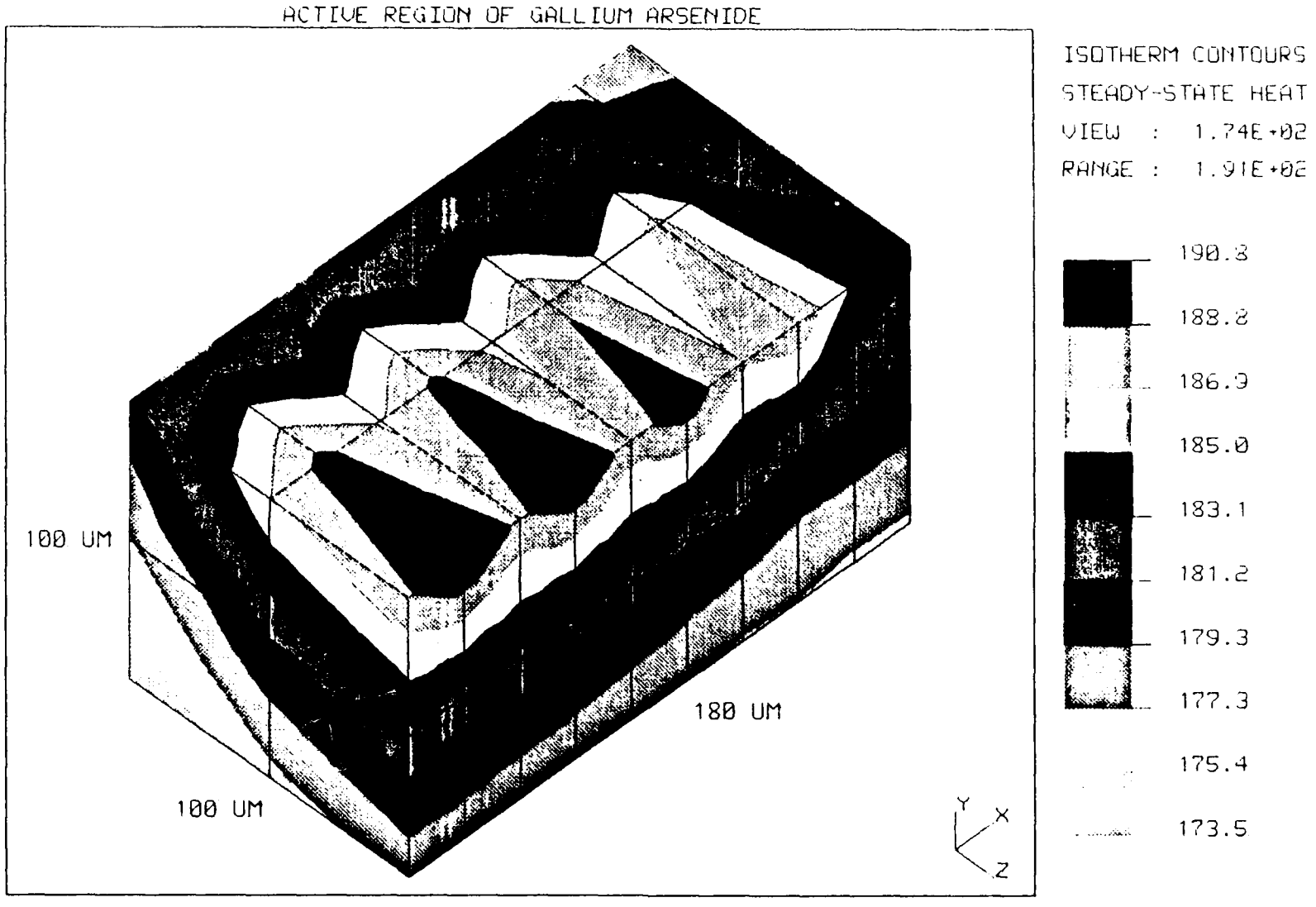


FIGURE 9: ACTIVE REGION GALLIUM ARSENIDE TEMPERATURES

Although there is a slight lowering of temperatures across the chip width (X-direction), one can assume adiabatic lines of thermal symmetry every 20 micrometers, especially toward the left side of the model (center of the actual chip). Therefore, one could model only 40 micrometers of chip in the X-direction which would include one half of a drain, one gate channel and one half of a source. The gate channel is 200 micrometers wide and because of symmetry, only one half (100 micrometers) needs to be modeled. 150 micrometers of material beyond the gate channel in the Z-direction (gate width direction) for a total of 250 micrometers is used as the Z-direction boundary. The entire 100 micrometer thickness of gallium arsenide, the 25 micrometer thick epoxy, and the 25 micrometer thick copper for a total of 150 micrometers of material is used as the Y-direction boundary. Thermal boundary conditions for the back and bottom planes are obtained from the prior one-quarter model simulation. Figures 10 and 11 show these boundary conditions for the back and bottom surfaces respectively. Initially elements of 5 micrometers in the X-direction are used, and finally, 1 micrometer wide elements are used in the space between the one-half drain and the one-half source. The 15 micrometer one-half drain, the 20 micrometer one-half source, and the 5 micrometer space between them accurately represent the device. One layer of gold elements, four layers of gallium arsenide elements, one layer of epoxy elements, and one layer of copper elements are used in the Y-direction. All elements are 25 micrometers in the Z-direction. Initially the source metal via was not modeled. Later the model was modified to include a 50 micrometer (Z-direction) via across the one-half source. Because of symmetry, this represents a via 100 micrometers long (Z-direction) by 40 micrometers wide (X-direction). The

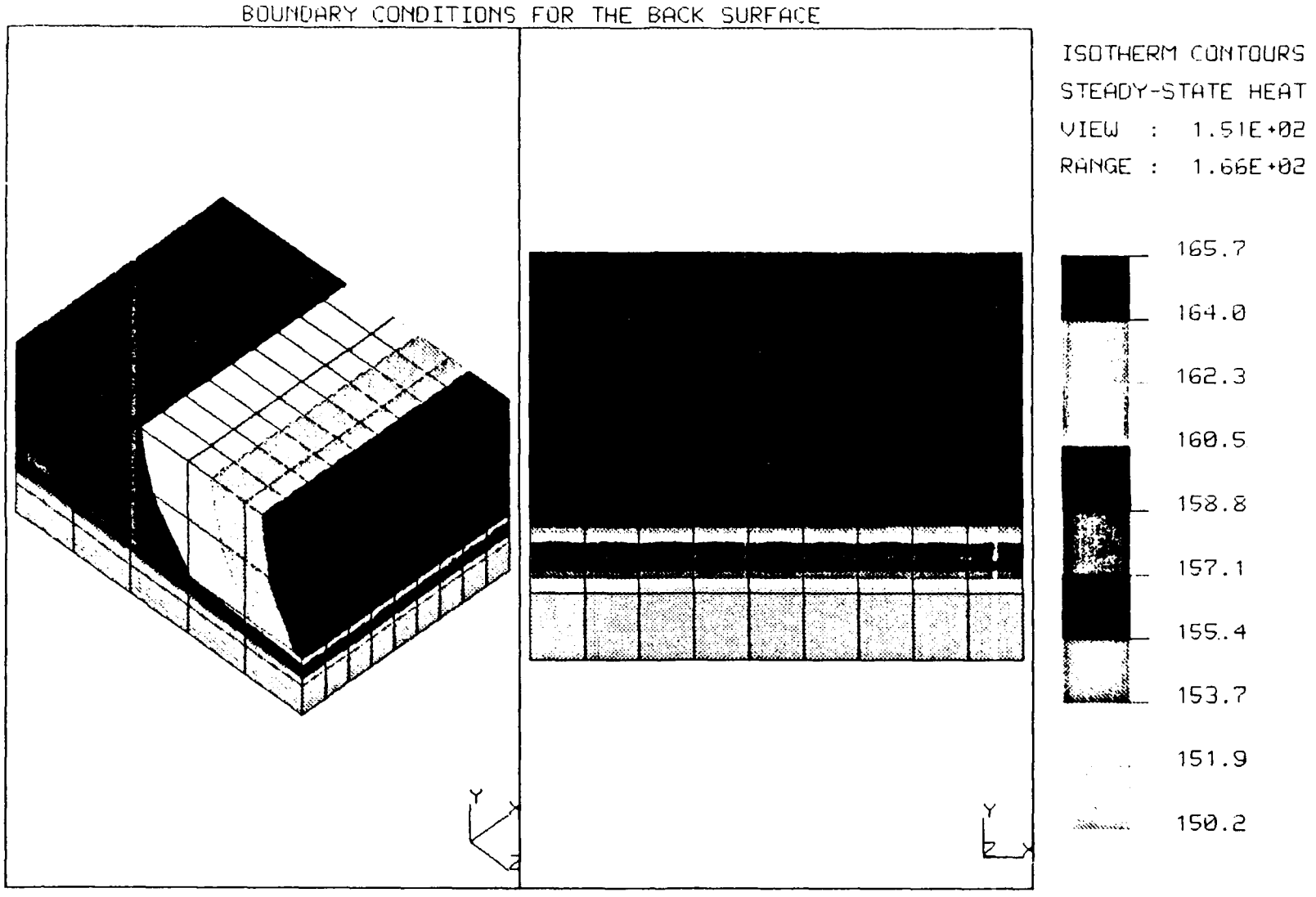


FIGURE 10: BACK SURFACE BOUNDARY CONDITIONS

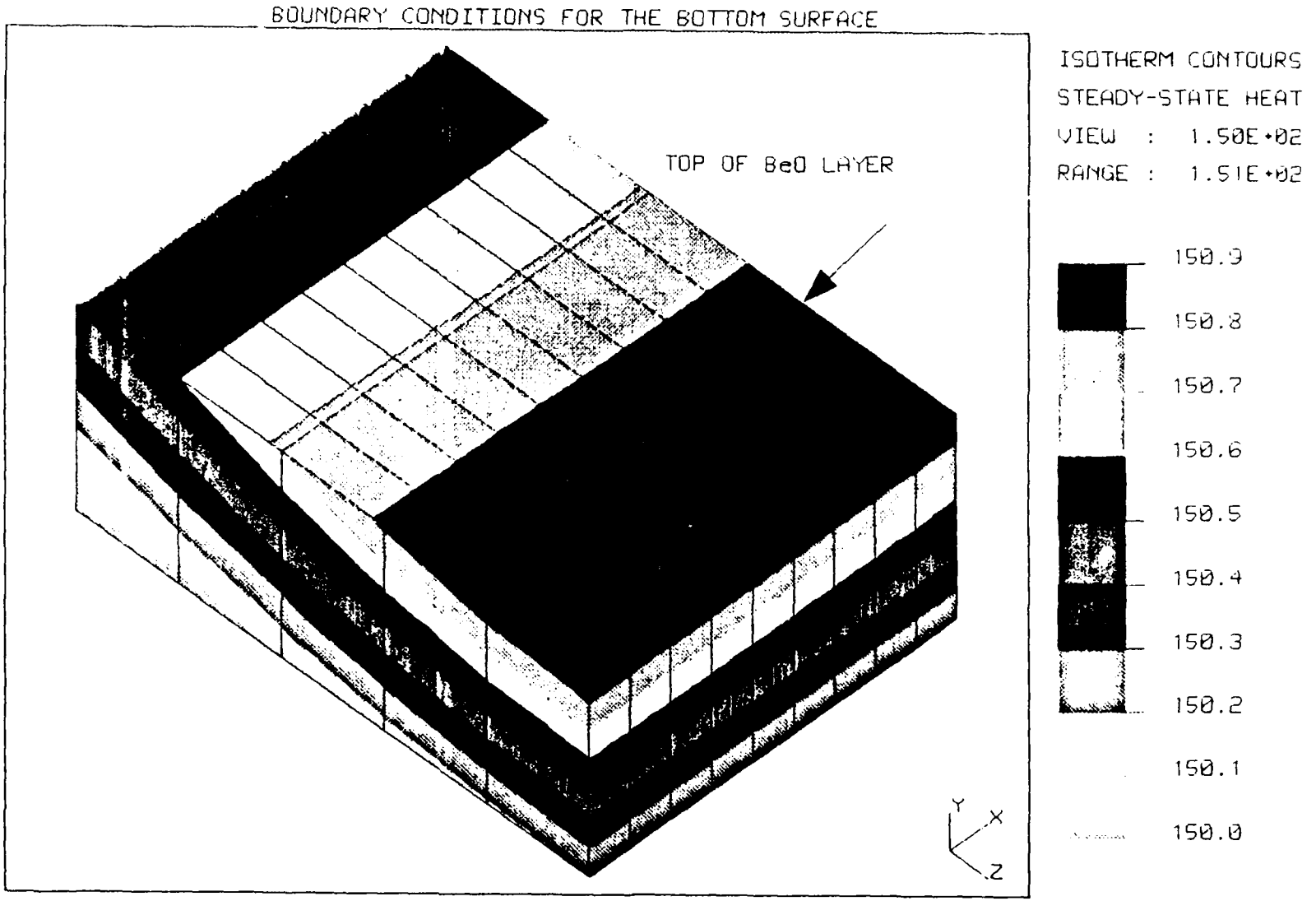


FIGURE 11: BOTTOM SURFACE BOUNDARY CONDITIONS

heat generation was simulated in several ways. They include:

1. Concentrated nodal heat inputs along lines on each side of the gate channel.

2. Internal element heat generation in the top layer of GaAs elements between the source and the drain (total material volume was 5 micrometers X 5.07 micrometers X 100 micrometers, X, Y, and Z directions respectively).

3. Distributed heat flux on the top surface of the same elements used in 2 above (5 micrometer X 100 micrometer area).

4. Distributed heat flux on the top surface of 1 micrometer wide elements midway between the source and drain (1 micrometer X 100 micrometer area).

Figure 12 shows the NISA finite element model and typical results, neglecting the source via. Table 2 summarizes the results for the four methods of heat generation. These results are somewhat unexpected in that they show nearly the same maximum temperature irregardless of the method of heat generation. The region of GaAs material where the heat is being generated is not as sensitive a parameter as might be expected. Thus it appears unnecessary to model the heat generation with cylindrical shaped elements. Accurate maximum temperature results can be obtained using either a flux loading on the top surface of the gate region, or as concentrated nodal heat inputs along each side of the gate channel. Interesting also is the agreement with results from the comparatively gross one-quarter cell model (190.8 for nodal heat generation and 191.1 for flux loading). Although the maximum temperature results are nearly the same for all of the simulations, the variation of temperature along the gate channel

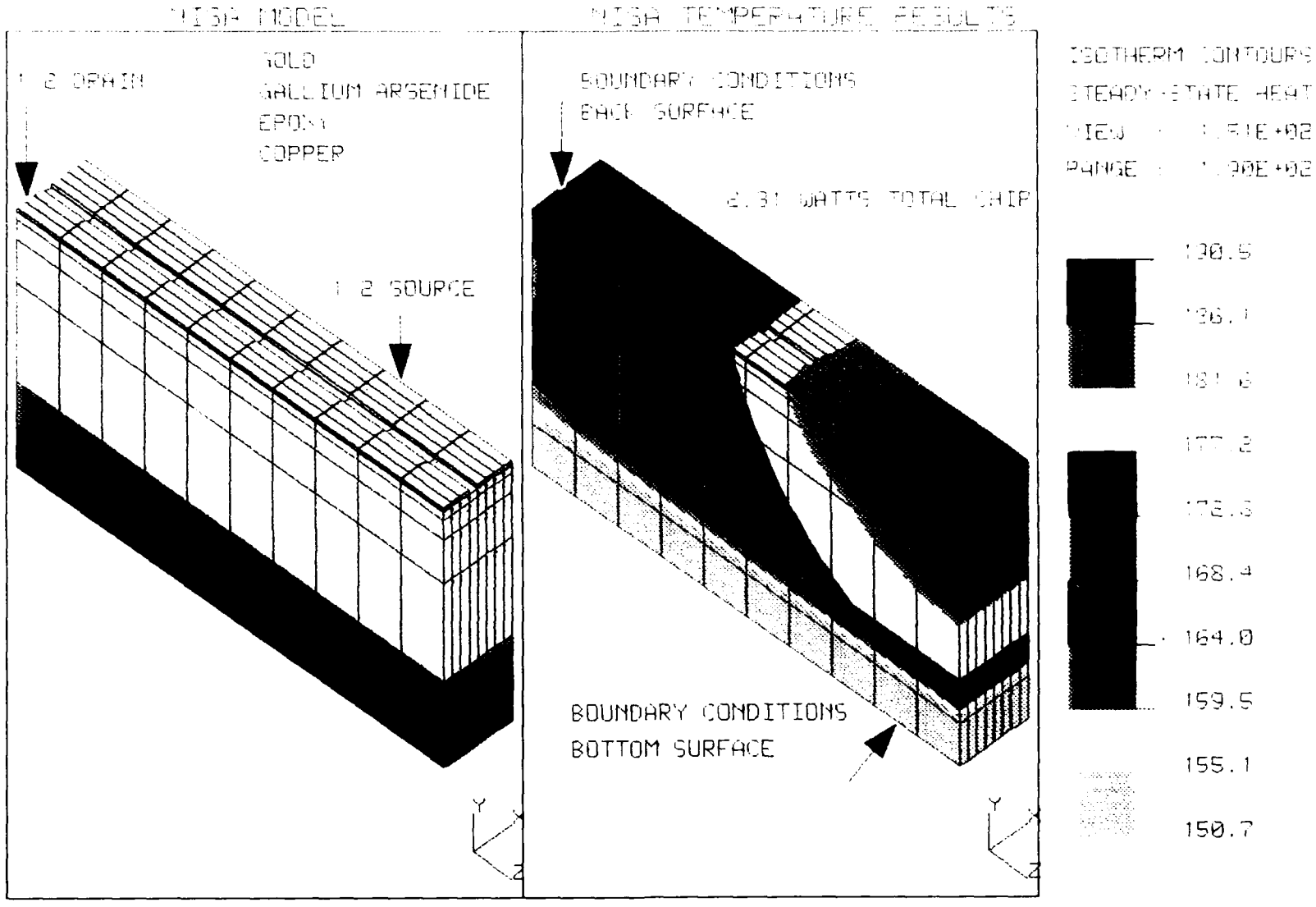


FIGURE 12: SINGLE GATE MODEL AND RESULTS

	METHOD	MAXIMUM TEMPERATURE (Degrees Centigrade)
1.	Concentrated Nodal Heat Input Along Each Side of Gate Channel	190.4
2.	Internal Element Heat Generation	189.8
3.	Distributed Heat Flux on Top Surface of GaAs (5 micrometer elements)	190.5
4.	Distributed Heat Flux on Top Surface of GaAs (1 micrometer elements)	193.3

TABLE 2 - SUMMARY OF HEAT GENERATION METHODS

length between the source and drain will best be determined with many small elements in the gate region. Figure 13 shows the temperature distribution with 5 micrometer wide elements. Figure 14 shows the overall model results and Figure 15 shows the temperature distribution for just the gate region of the GaAs when 1 micrometer wide elements are used for heat generation. Figures 16 and 17 show the same results when the source via is modeled. Again, the agreement with the one-quarter cell model is surprising (184.9 vs. 185.5 for the one-quarter model). The largest of these models, the one shown in Figure 14, contained 790 elements and 1100 nodes. The results shown in Figure 15 provide the most accurate variation of temperatures across the gate channel of a FET under steady state conditions. The results in Figure 17 provide the largest expected temperature difference between the drain and source of a FET under steady state conditions.

3.0 2-D VS. 3-D ANALYSES

3-D models are more difficult to develop, contain more elements and nodes, and require longer computer run times than 2-D models of the same overall dimensions. 2-D models are used whenever possible, especially for transient simulations where many heat balance computations are performed. A 2-D simulation in the X-Y plane assumes that there is no heat transfer in the Z-direction. For zero heat transfer there should be no thermal gradient in that direction. This requires the heat to be generated uniformly along the third dimension. A typical 2-D simulation of the chip would consider the cross-section through the two FET cells along the chip width direction (narrowest dimension with the cells closest together). A 2-D analysis corresponding to the simulation described in Section 2.0 is made. The 3-D results are shown in Figure 4. The heat for the 2-D simulation is

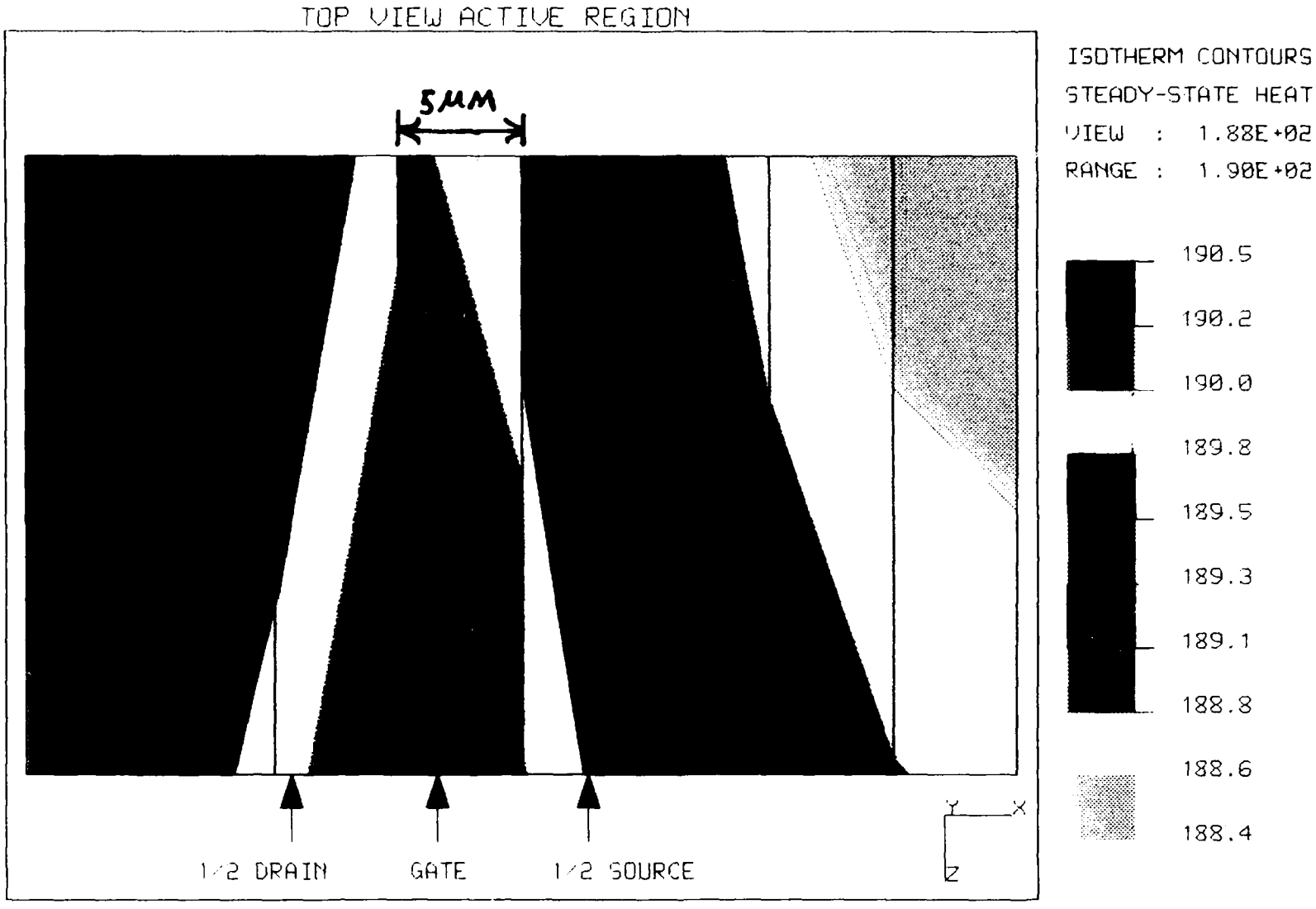


FIGURE 13: SURFACE TEMPERATURES USING 5 μM ELEMENTS

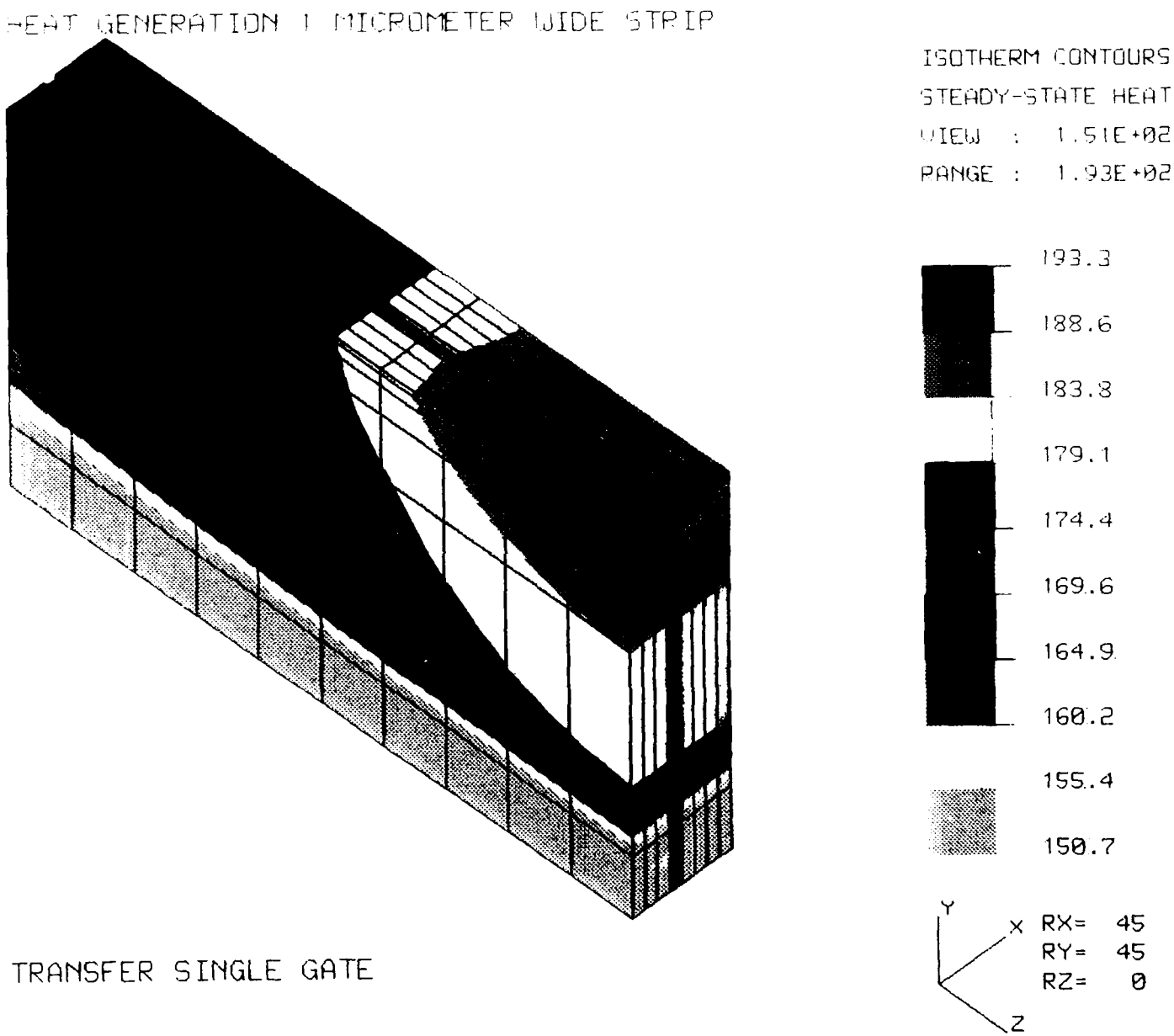


FIGURE 14: SINGLE GATE MODEL & RESULTS USING 1 μM ELEMENT

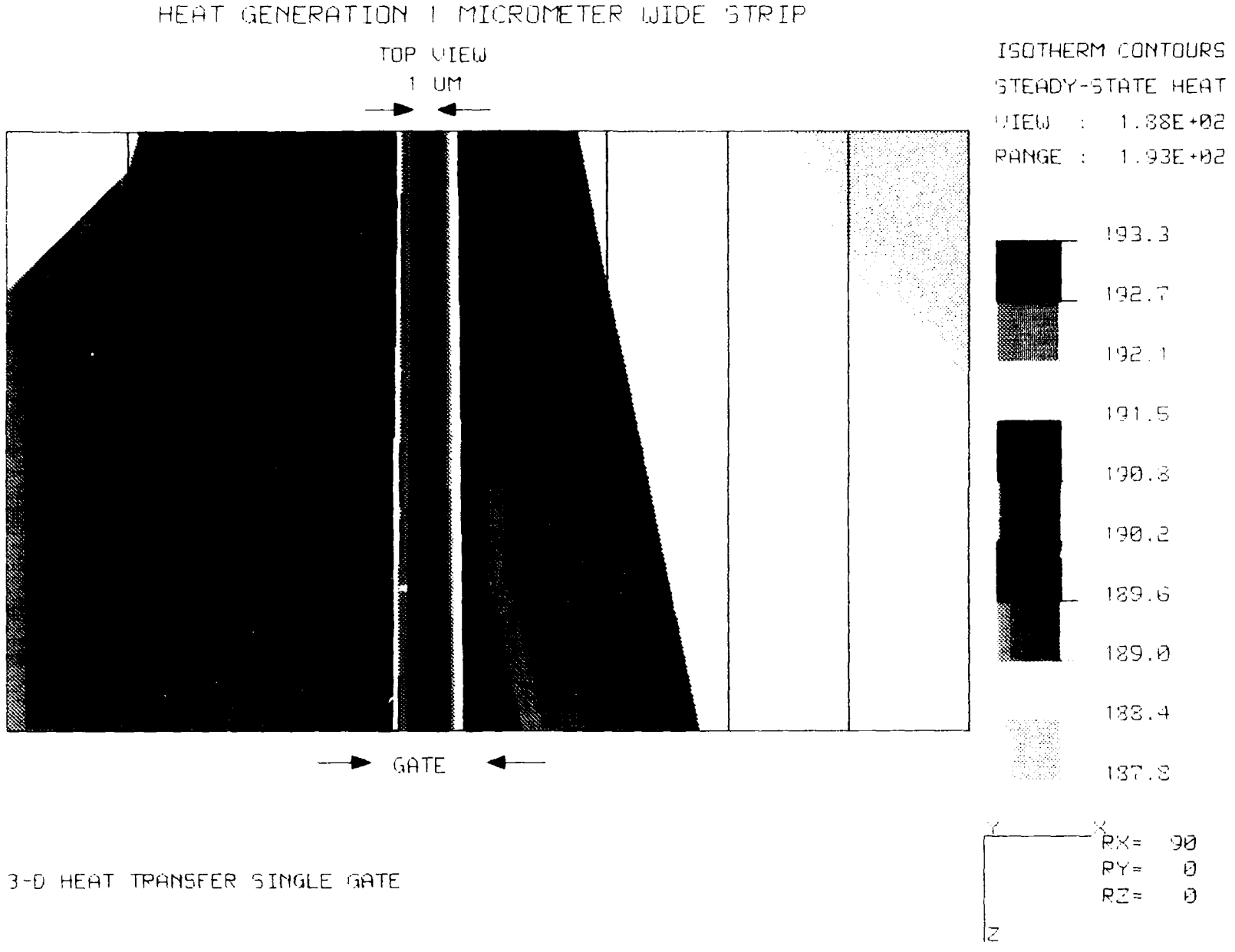
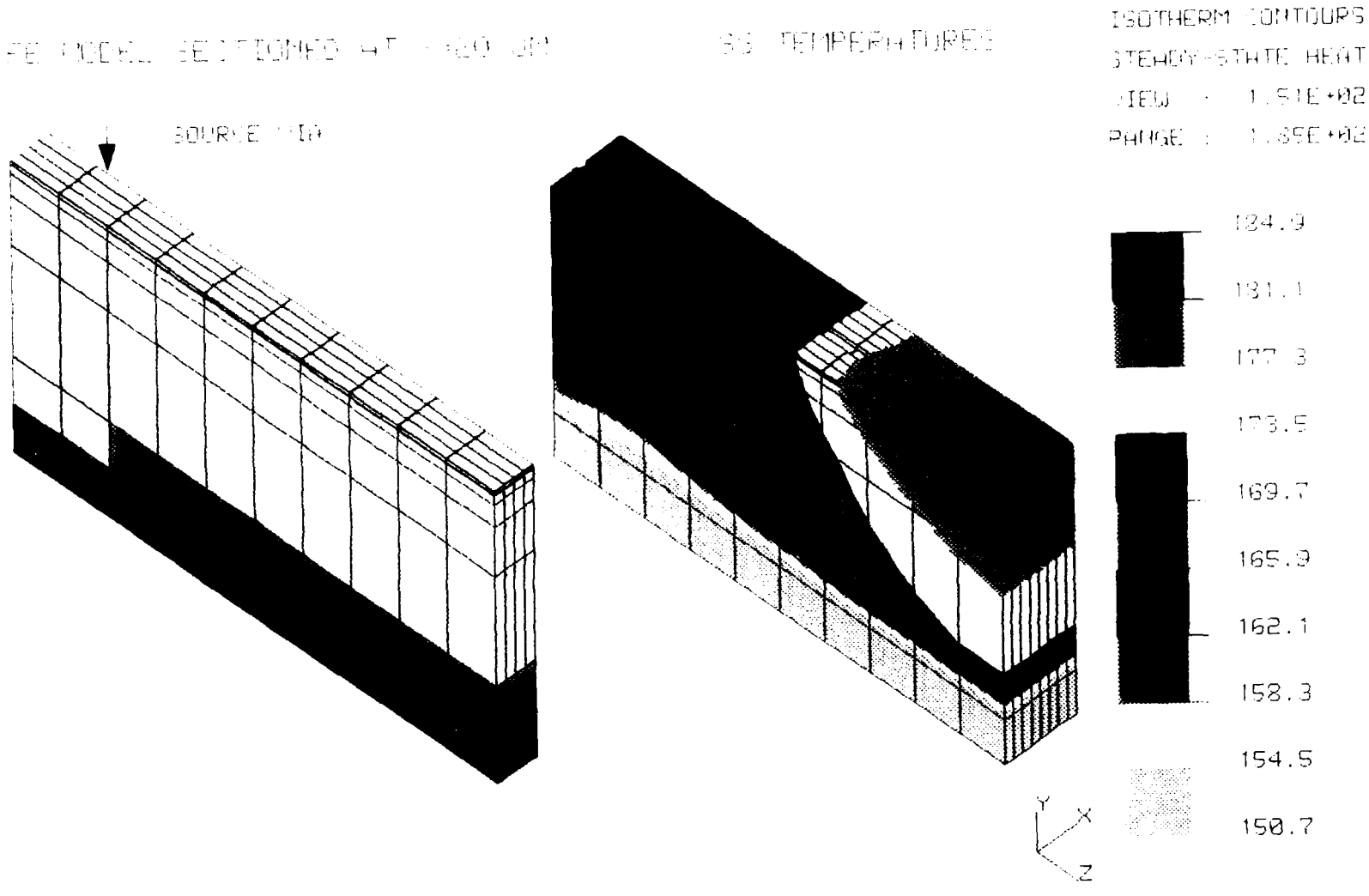


FIGURE 15: SURFACE TEMPERATURES USING 1 μM ELEMENTS



3-D HEAT TRANSFER SINGLE GATE WITH SOURCE VIA

FIGURE 16: SINGLE GATE WITH METALLIZATION

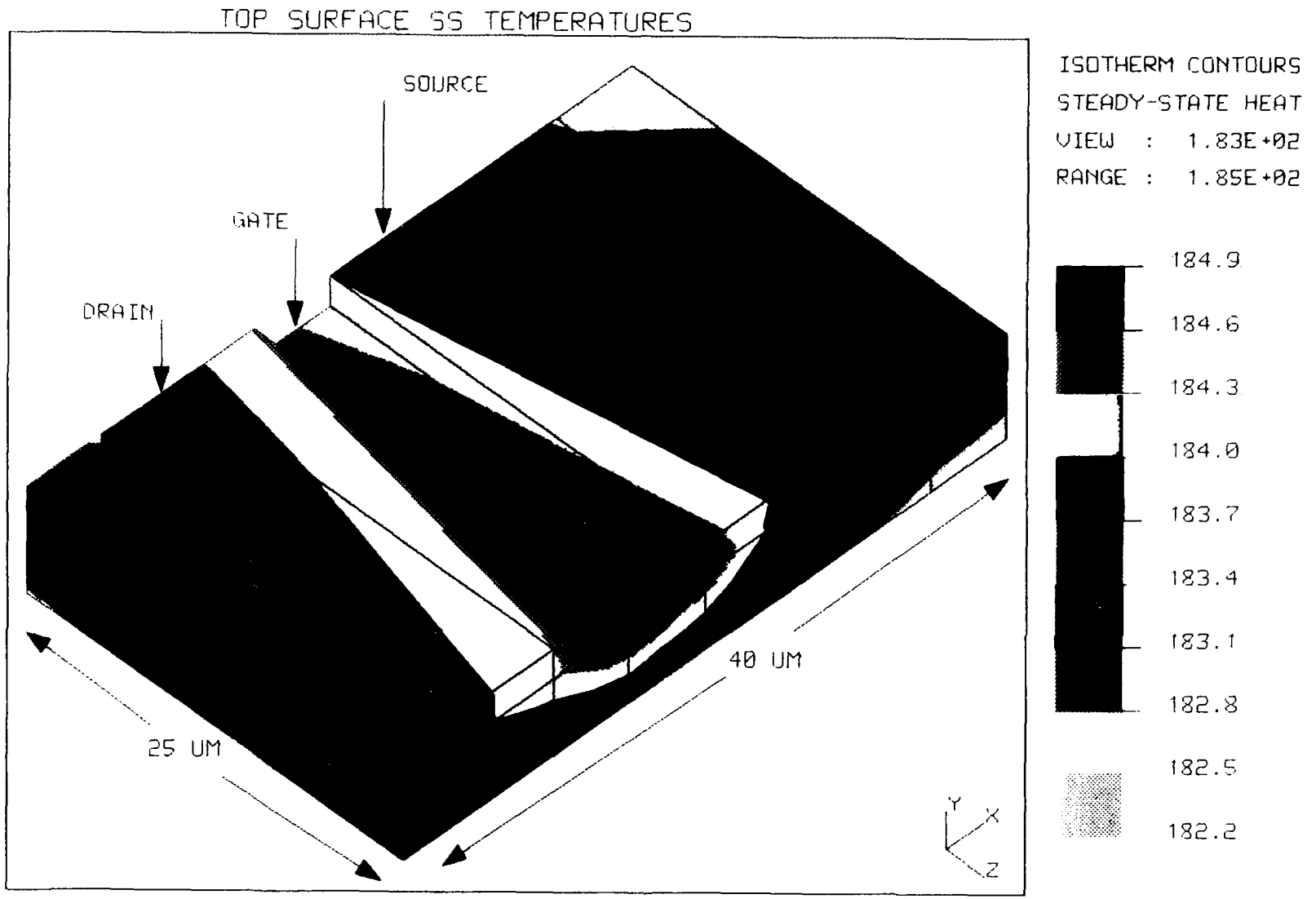


FIGURE 17: SURFACE TEMPERATURES WITH METALLIZATION

generated as a flux on the top surface of the two elements that represented each active region. Each active region is 250 micrometers across. The elements are 125 micrometers wide. The heat rate is calculated as follows:

2.31 watts/chip X 1 chip/6cells = .385 watts/cell

.385 watts/cell X 1 cell/250 X 250 square micrometers =

6.16×10^{-6}/watts/square micrometer

Recall the 3-D chip model used an active area of 250 micrometers X 250 micrometers. For a 2-D simulation, the heat is generated per unit depth in the Z-direction. Therefore, the heat generation rate is:

6.16×10^{-6} watts/square micrometer X 1 micrometer deep =

6.16×10^{-6} watts/micrometer

This is the rate per unit dimension in the X-direction. Figure 18 shows the 2-D simulation results. The maximum chip temperature is 170.6 vs. 137.2 for the 3-D analysis. Therefore, neglecting heat transfer along the "gate width" direction of a transistor chip results in temperatures considerably higher than a 3-D simulation would provide.

3.1 IMPROVED 2-D MODELS AND ANALYSIS

Studying the results of the 3-D chip model shown in Figure 4, the thermal gradient in the Z-direction can be seen to be significant (137.2 to 100). However, the gradient in the X-direction for the two cells that are close together is less (137.2 to approximately 116). This condition is closer to the assumptions necessary for an accurate 2-D simulation discussed in Section 3.0, namely, a uniform temperature in the third direction. Figure 6 for the 3-D model of one-quarter of a FET cell also shows a small gradient in the X-direction compared to the gradient in the Z-direction. Therefore, if one were to section the chip in the Y-Z plane

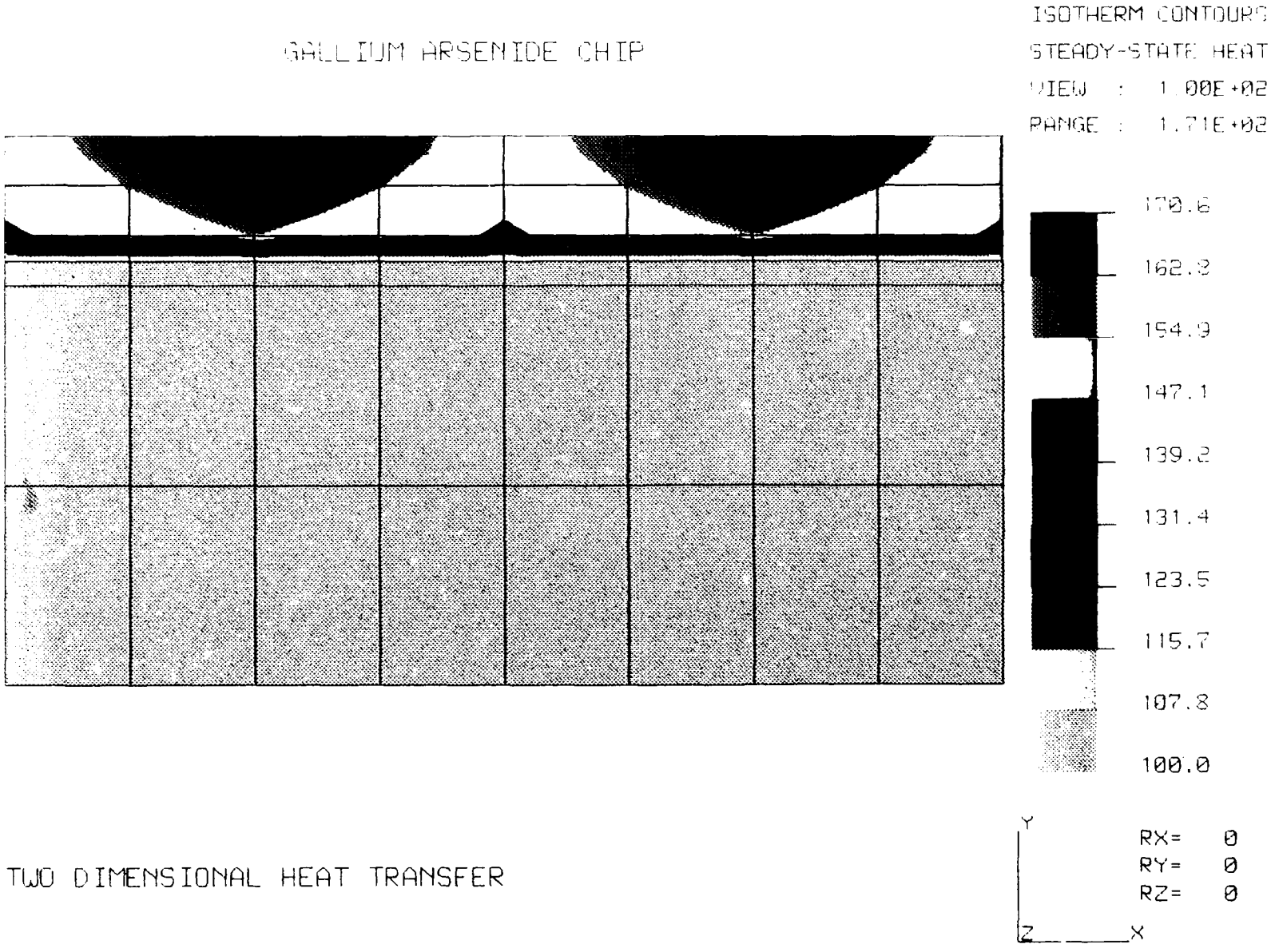


FIGURE 18: 2-D SIMULATION RESULTS

(chip length and gate width directions), better results would be expected. The same 2-D model described in Section 3.0 was used and several analyses were performed. First, the heat was generated using the same 6.16×10^{-6} watts/micrometer on the top surface of the two center elements with adiabatic surfaces on both sides of the model (no heat transfer beyond 500 micrometers of material on each side of the center of the active region). This produced a maximum temperature of 154.8, which is better than before (170.6), but still much higher than the 3-D result of 137.2. Next, using boundary conditions from the results of the 3-D analysis, first one side, then both sides of the 2-D model were specified. Those results produced maximum temperatures of 168.4 and 156.6 respectively. Placing boundary conditions on surfaces or edges that are adiabatic should not be done. A procedure not tried, but one that would result in low temperatures, would be to consider the 2-D plane to pass between the two cells and to determine the heat generation rate by dividing the heat produced in two cells (.77 watts) by the total area across the entire width of the half chip (1000 micrometers X 250 micrometers). This would give a heat generation rate of 3.08×10^{-6} instead of 6.16×10^{-6}. The best procedure is to start with a 3-D model of a relatively large region, then use the 3-D results for the boundary conditions of a refined, small region, 2-D model. The 2-D model to demonstrate this procedure will consider the same amount of material as was used for the 3-D single gate model described in Section 2.4, i.e., 250 micrometers in the gate width direction (now the X-dimension) and the same 100 micrometers of GaAs, 25 micrometers of epoxy, and 25 micrometers of copper for a total of 150 micrometers of material in the Y-direction. The 2-D model is shown in Figure 19 and is a 2-D representation of a 3-D model.

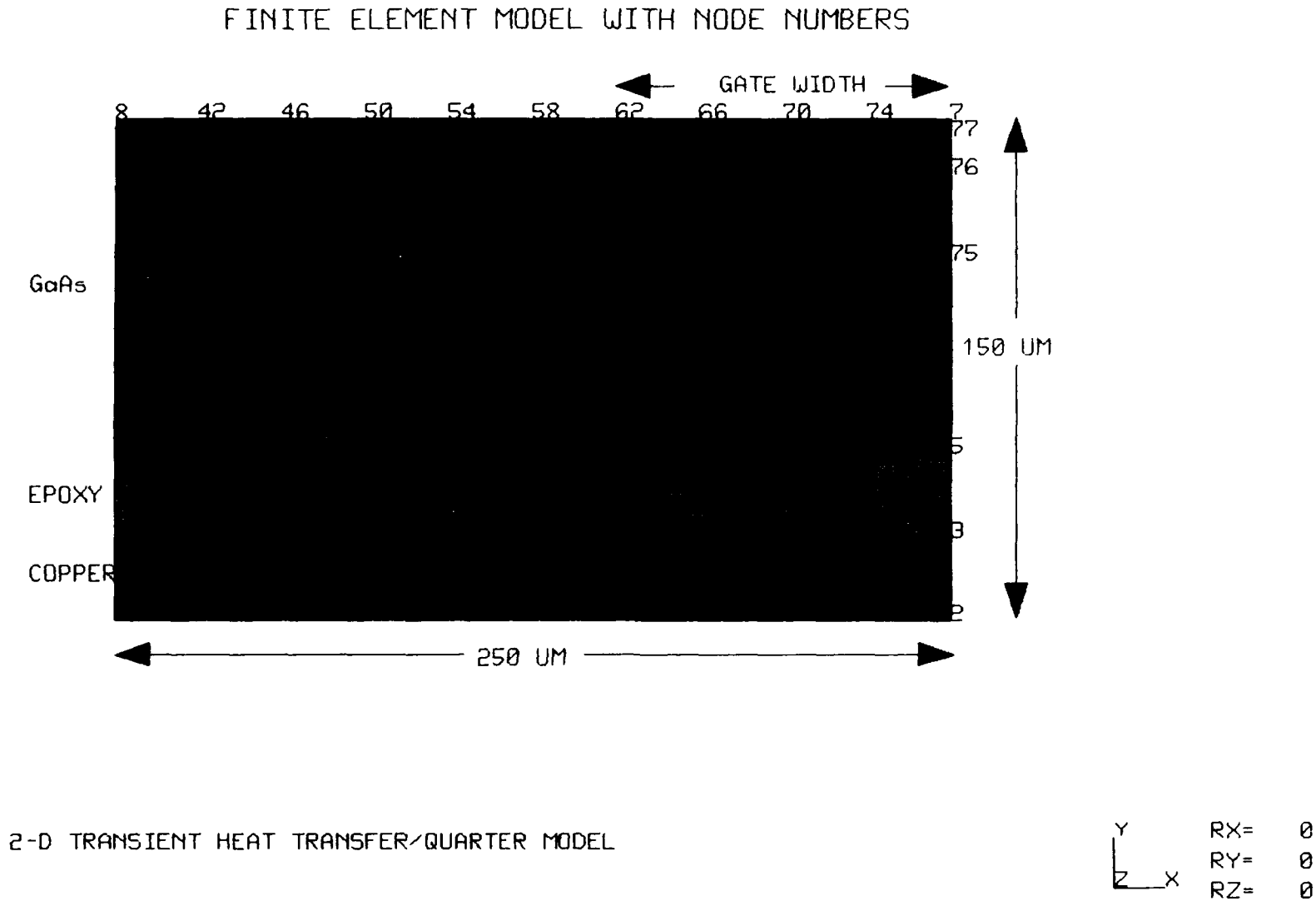


FIGURE 19: 2-D MODEL REPRESENTATION OF 3-D QUARTER CELL

Note that node 7 at the upper right corner of the model represents the center of the gate region of the actual FET cell. Boundary conditions for the bottom and side nodes are obtained from the 3-D, one-quarter model and are shown in Figures 20 and 21 respectively. Two methods of heat generation are used, and are described as follows:

A. Heat Flux

The same uniform heat flux as was used for the 3-D, one-quarter FET cell model will be used.

2.31 watts/chip X 1 chip/6cells X 1/4 of a cell = .0963 watts

.0963 watts/100 X 120 square micrometers = 8.025×10^{-6} watts/square micrometer

The quarter model used an active area 120 micrometers long. A 2-D model uses elements with a unit thickness. Therefore, the heat flux is 8.025×10^{-6} watts/micrometer.

B. Concentrated Nodal Heat Input

Although one-quarter of a FET cell dissipates .0963 watts, the 2-D model considers only a 1 micrometer deep slice out of the 3-D device, and it would be incorrect to consider a total nodal heat load of .0963 watts. A 1 micrometer slice has a total heat input of:

8.025×10^{-6} watts/square micrometer X 1 micrometer depth X 100 micrometer width = 8.025×10^{-4} watts

The nodal heat loads are determined by dividing the total heat load of 8.025×10^{-4} watts by the four elements representing the heat generation region, and apportioning the element load to the appropriate nodes.

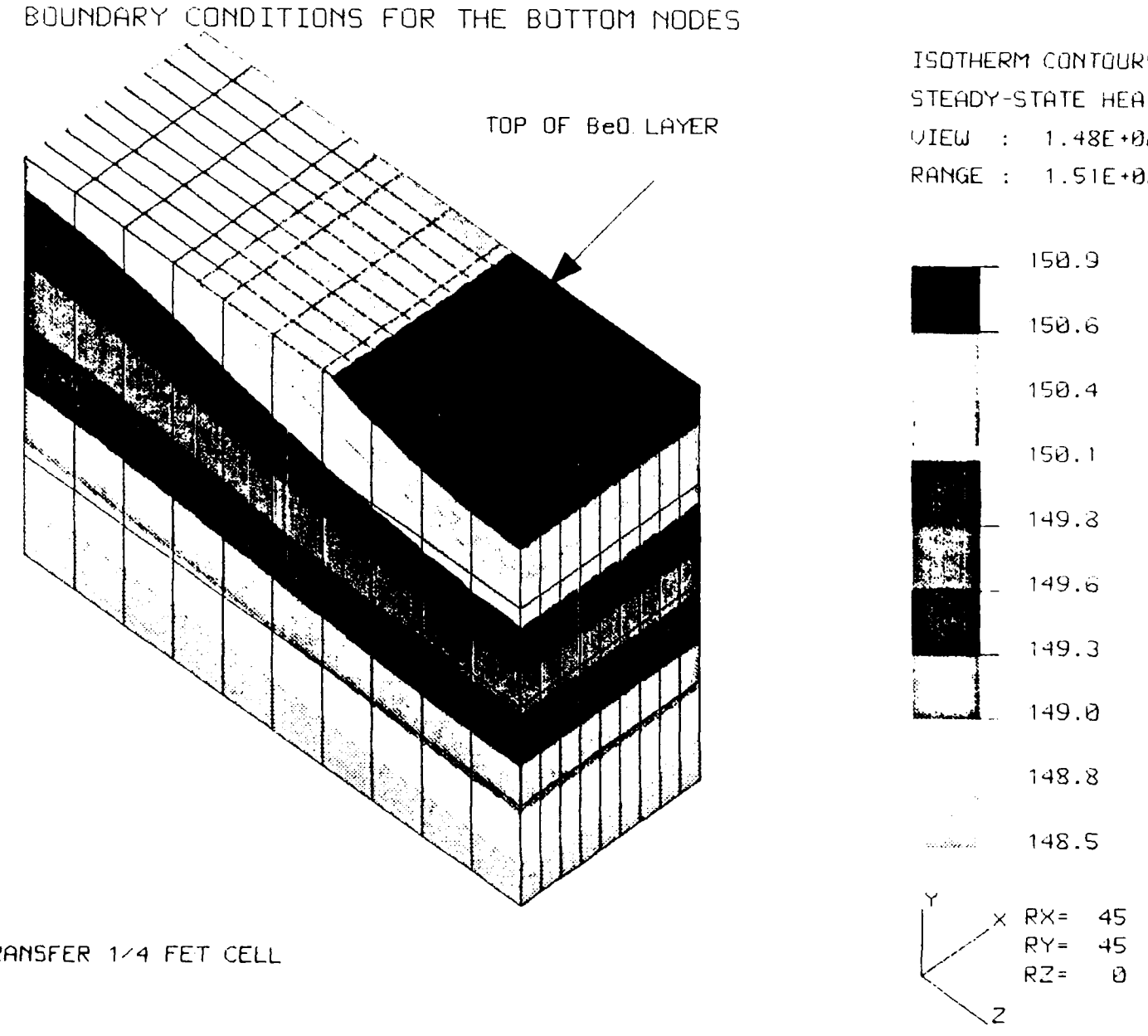


FIGURE 20: BOTTOM NODE BOUNDARY CONDITIONS

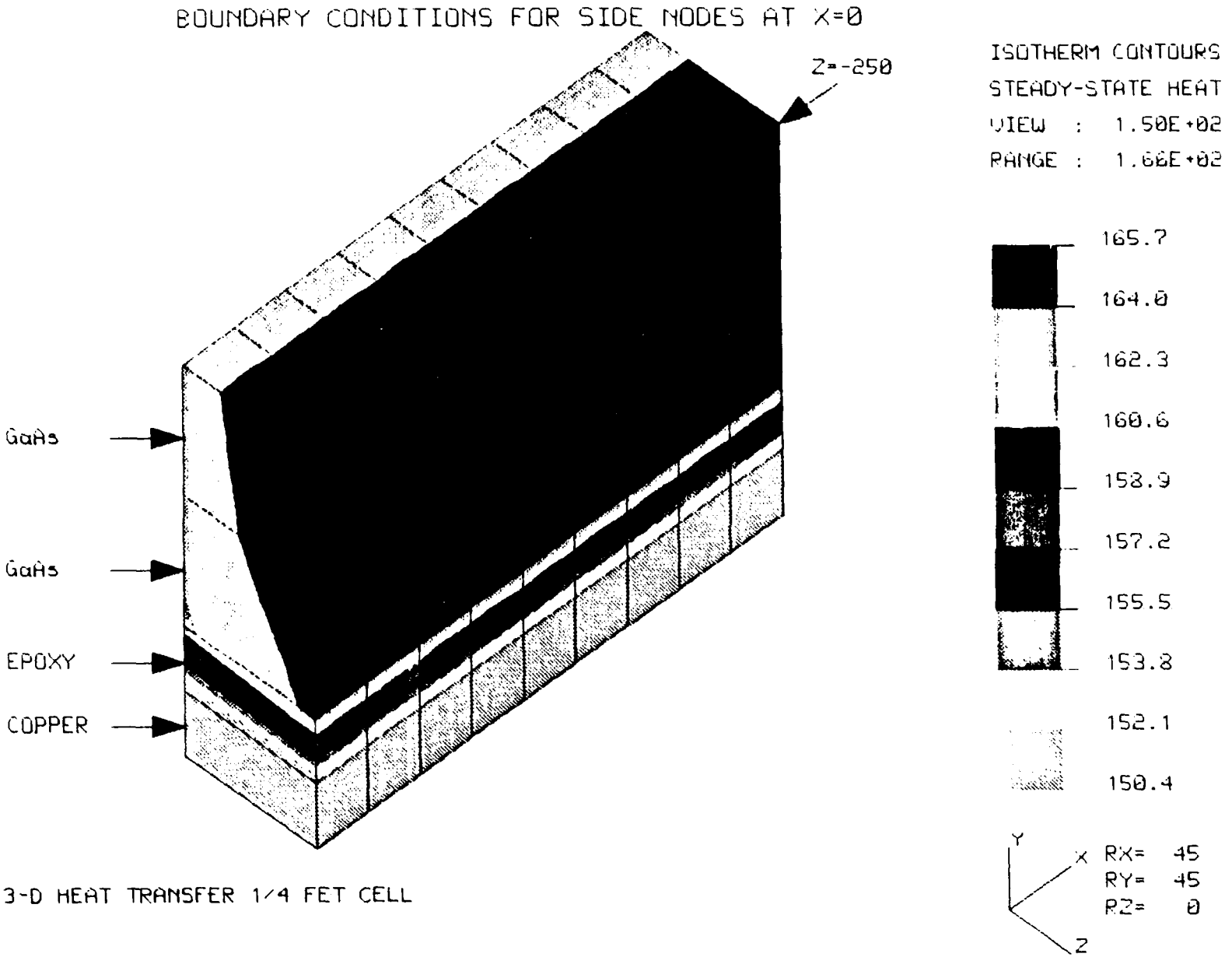


FIGURE 21: SIDE NODE BOUNDARY CONDITIONS

For the nodes shown in Figure 17, the nodal heat loads are:

Nodes 7 and 62 - 8.025×10^{-4} watts/4 elements X 1/2 = 1.003×10^{-4} watts

Nodes 74, 70, 66 - 8.025×10^{-4} watts/4 elements = 2.006×10^{-4} watts

Both methods of heat generation produced the identical result, a maximum temperature of 202.0 degrees. Figure 22 shows the temperature contours. The maximum temperature for the 3-D analysis of a single gate was 190.5 degrees (heat flux with 5 micrometer wide elements, no source via). Thus the 2-D simulation results in a temperature difference from heat sink to gate channel of 102 degrees, 13% higher than the 3-D simulation result.

Although a 13% difference is not great, 2-D simulations of transistor chips are not recommended. Figure 4 clearly shows thermal gradients in all three directions. However, the closer together the transistor cells become, the better the assumption of a uniform heat dissipation and a uniform temperature distribution between the cells. Furthermore, care must be taken when determining the magnitude of heat application. One should visualize the 3-D region that the 2-D model will represent, and first calculate the heat per unit area that is generated in the appropriate area of the 3-D region. The heat generation for the 2-D model will be the heat per unit depth of a thin slice through the 3-D region. The numerical value of heat flux for the 2-D simulation (watts per unit length) will be the same as the numerical value of heat flux if a 3-D simulation were performed (watts per unit area).

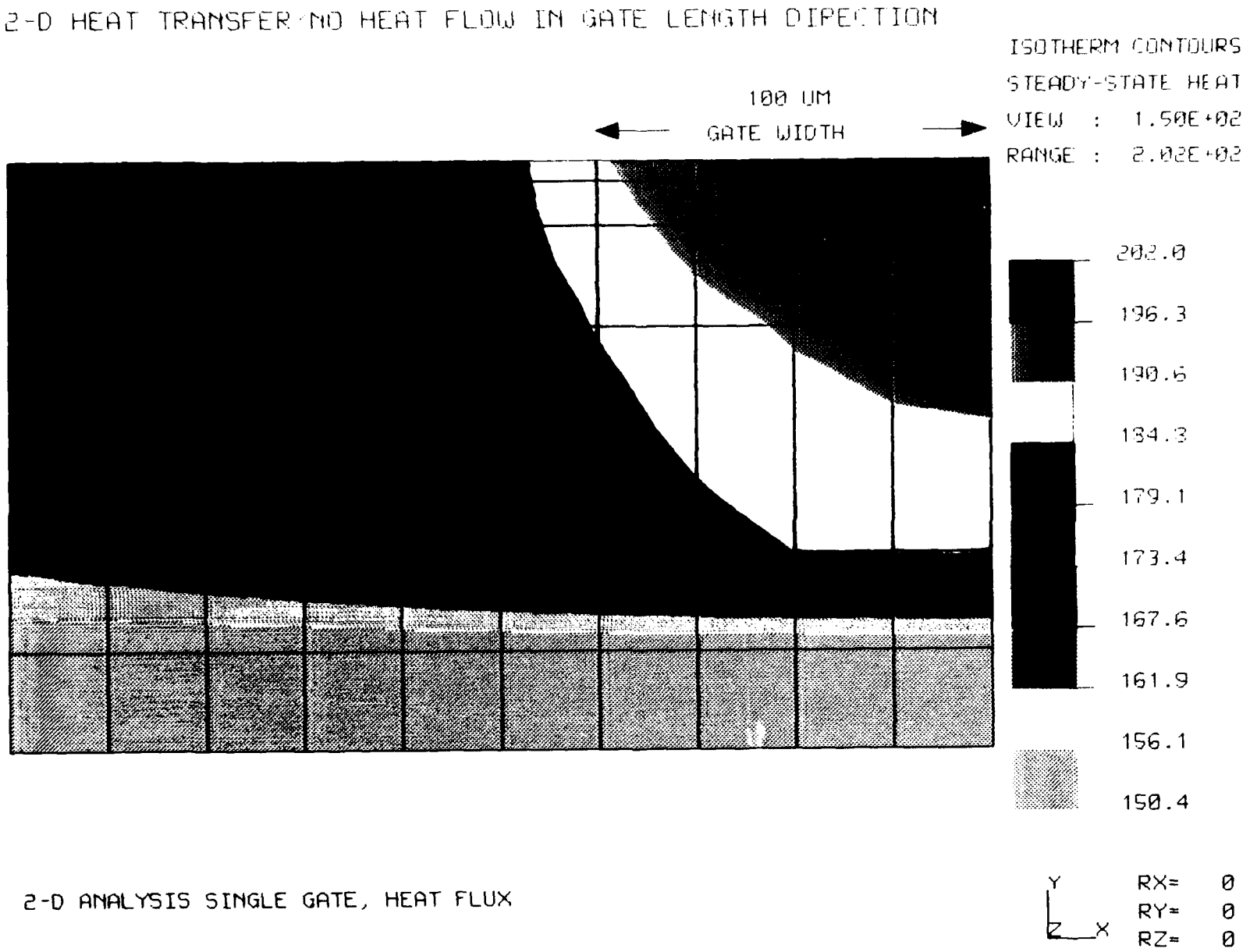


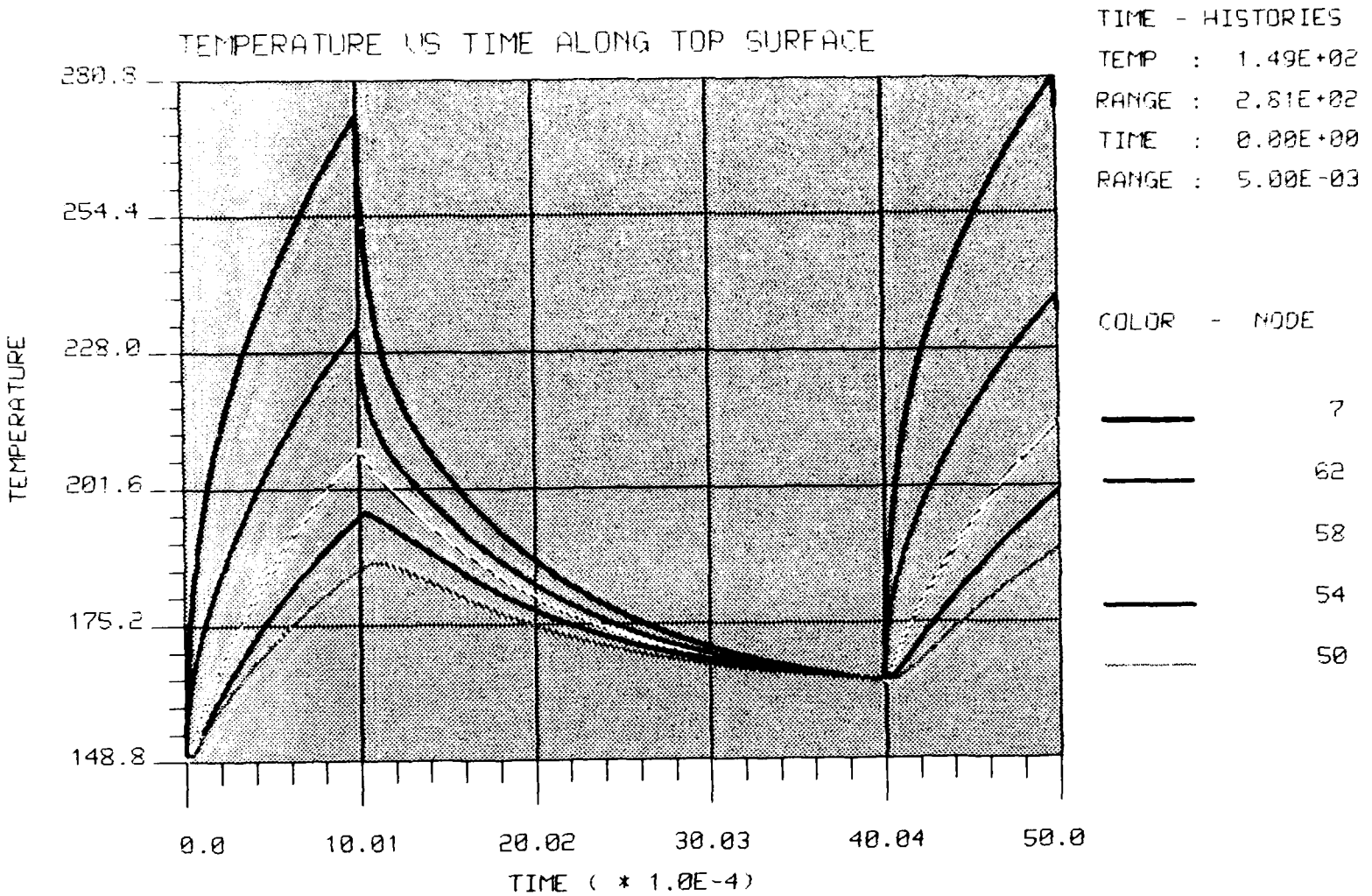
FIGURE 22: IMPROVED 2-D MODEL TEMPERATURE RESULTS

4.0 TRANSIENT SIMULATIONS

The pulsed operation of the C-band module driver amplifier causes a time variant heat generation and results in temperatures that vary with time as well as temperature variation throughout the device. The time variant heat generation can be simulated by performing finite element transient heat transfer analysis. The transient analysis requires the nodal heat balance equations to be solved numerous times at a selected time step interval. The objectives for performing a transient simulation are:

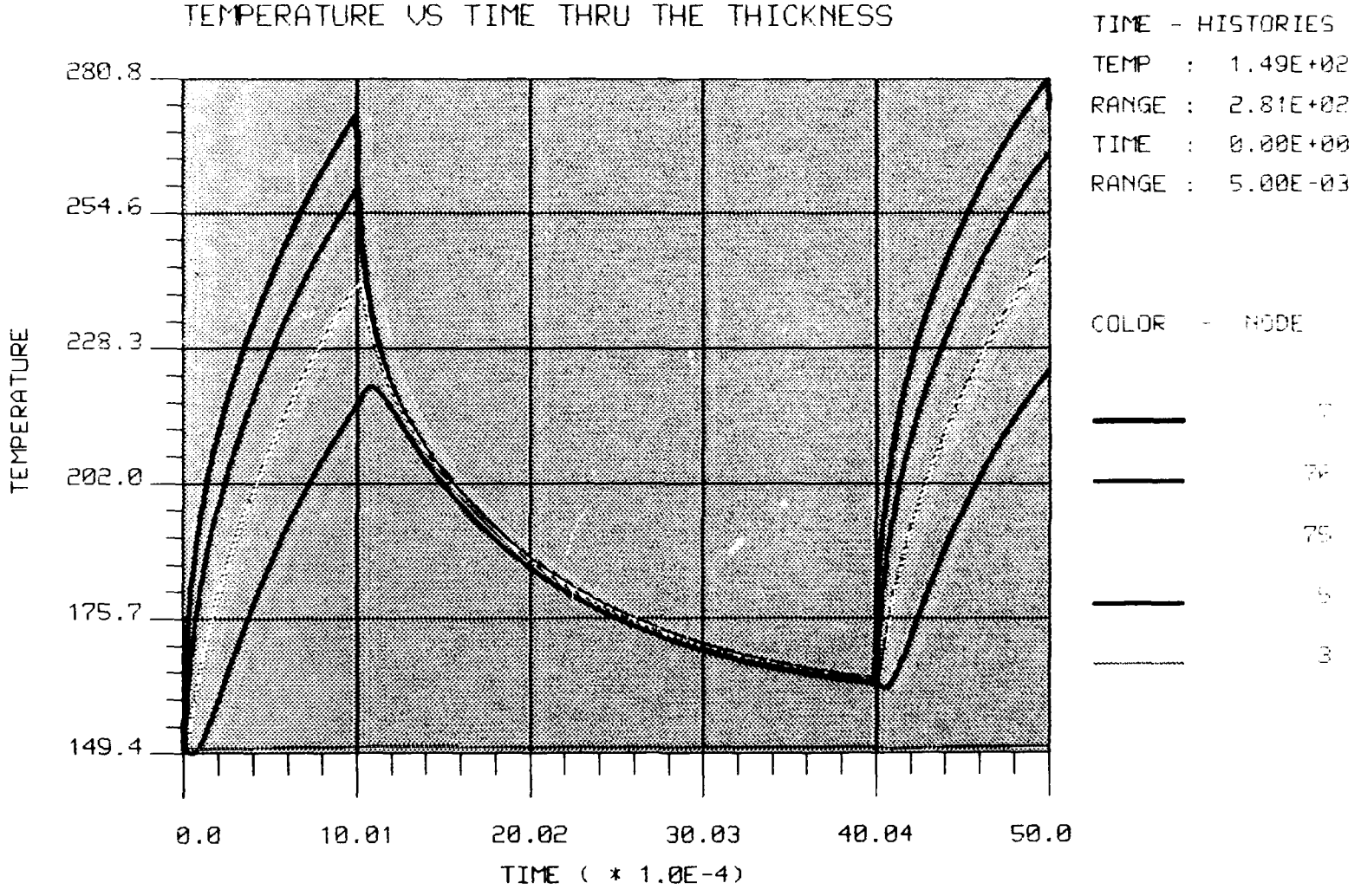
1. To determine the variation of temperature with time to obtain peak temperatures
2. To compare transient results with steady state results that use an appropriate duty cycle
3. To determine the distance away from the active region on the chip where the temperatures remain fairly constant with time and thus to know where infrared measurements will be able to follow dynamic behavior.

The first transient simulations are performed using a 2-dimensional model. Certain test runs are required that could best be performed with a smaller model. In particular, the time step for the analysis was varied. The 2-D model used is the same as the model used for the steady state analysis and is shown in Figure 19. The amplifier operates for a 1 millisecond long pulse separated by 3 millisecond intervals between pulses. The duty cycle = 1/(1+3) = .25 = 25%. The peak heat = 2.31 watts/.25 = 9.24 watts. A total time interval of 5 ms containing two pulses was simulated. A time step of 5×10^{-6} seconds was selected for a total of 1,000 calculations over the 5 ms time interval. Figures 23 and 24



2-D TRANSIENT HEAT TRANSFER/QUARTER MODEL

FIGURE 23: 2-D MODEL TRANSIENT RESULTS ALONG TOP SURFACE



2-D TRANSIENT HEAT TRANSFER/QUARTER MODEL

FIGURE 24: 2-D MODEL TRANSIENT RESULTS THROUGH THE THICKNESS

show the temperature vs. time results. Figure 25 shows the temperature contours at a particular time - in this case, at the end of the second pulse at 5 ms. Recall that the maximum steady state temperature, at node 7, was 202 degrees. Also, recall that steady state boundary conditions were applied at the bottom and the left side surfaces of the model. Figure 26 shows the onset of numerical instability when an improper time step is used. Figure 27 shows the response for six pulses and confirms that after two pulses the maximum temperatures have been reached. Figure 28 shows the reaction to one long pulse at a 25% duty factor and indicates that after 6 ms, steady state conditions would be reached. The significance of this result is that the 1 ms pulse for this device is short and there is not enough time for the circuit to reach even higher temperatures than the 280 degrees indicated in the multiple pulse simulations. A longer pulse time would result in even higher temperatures.

4.1 3-DIMENSIONAL TRANSIENT SIMULATION

A 3-dimensional simulation is performed using the one-quarter of a FET cell model. This model is selected because it models a relatively large region of the chip and also because the only boundary conditions applied are for the heat sink at the bottom of the mount. The model and steady state results are shown in Figure 6. The transient temperature vs. time results are shown in Figures 29 and 30. The nodal locations are along the top of the chip and start with node number 1610 at the center of a cell (right edge of the finite element model). Nodes 1610 and 1614 are along a gate line between a source and a drain. The distances from the center of a cell, along the top surface of the chip, for each node identified in

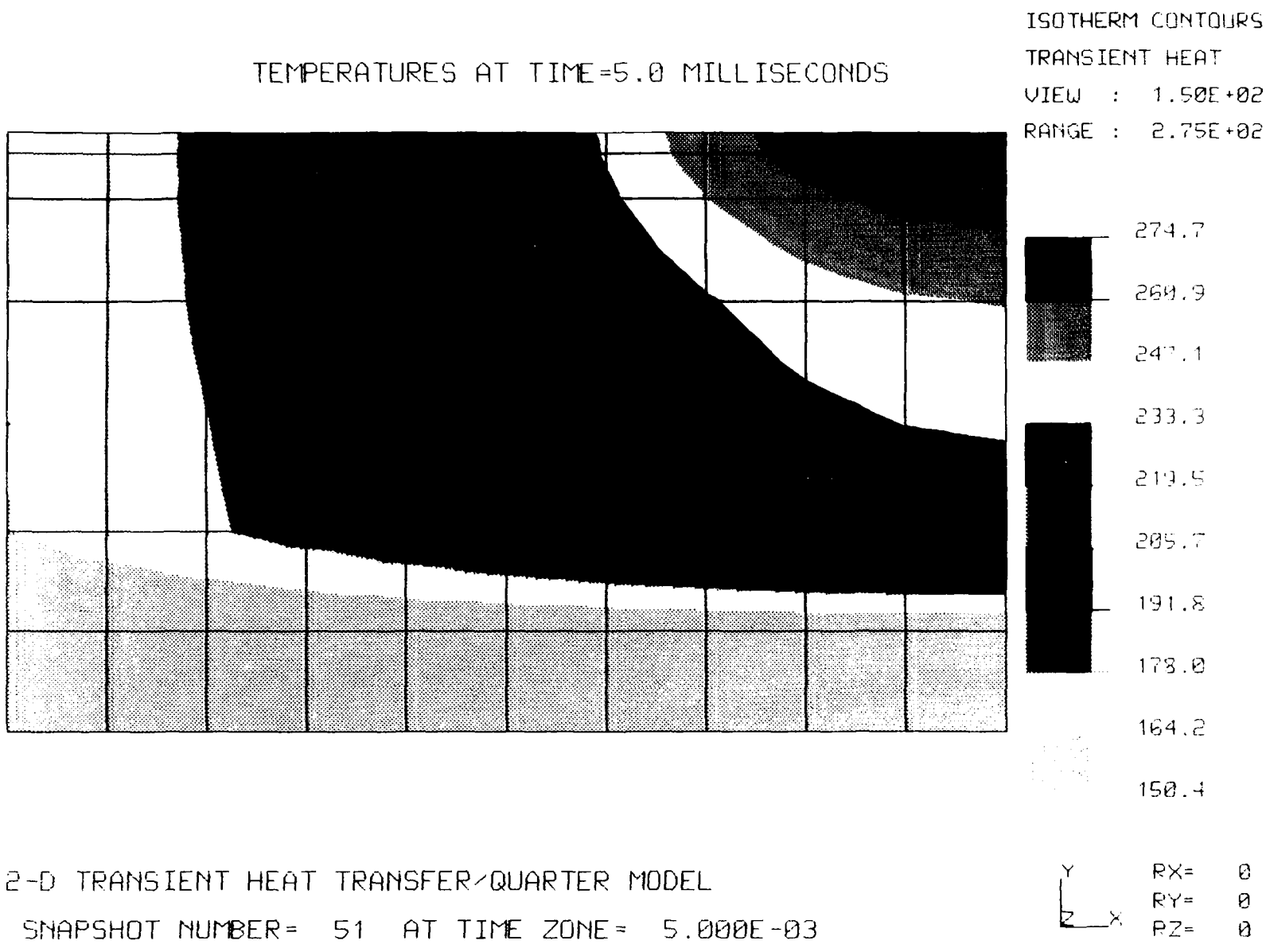


FIGURE 25: 2-D MODEL TRANSIENT TEMPERATURES AT 5 MS

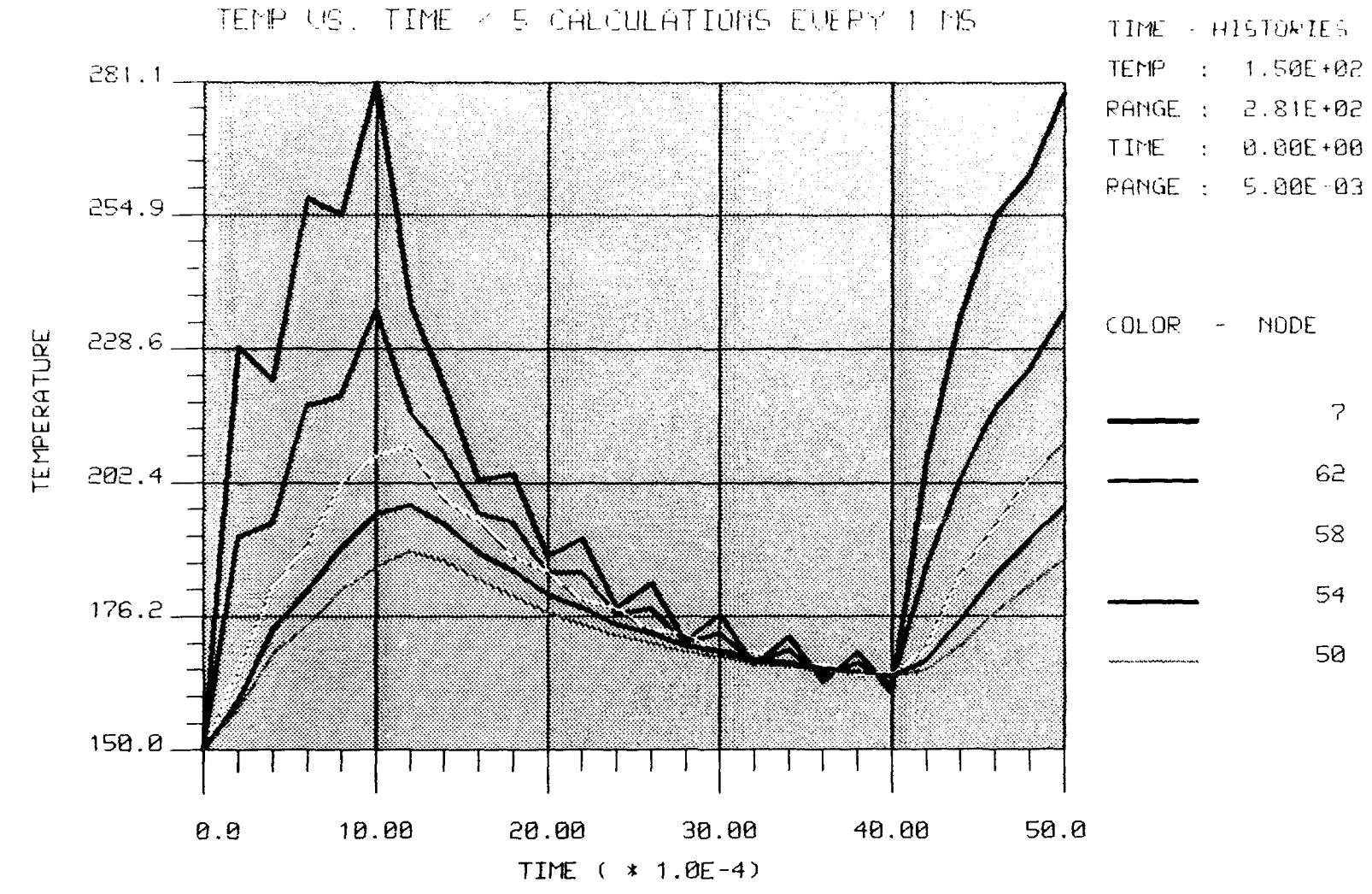
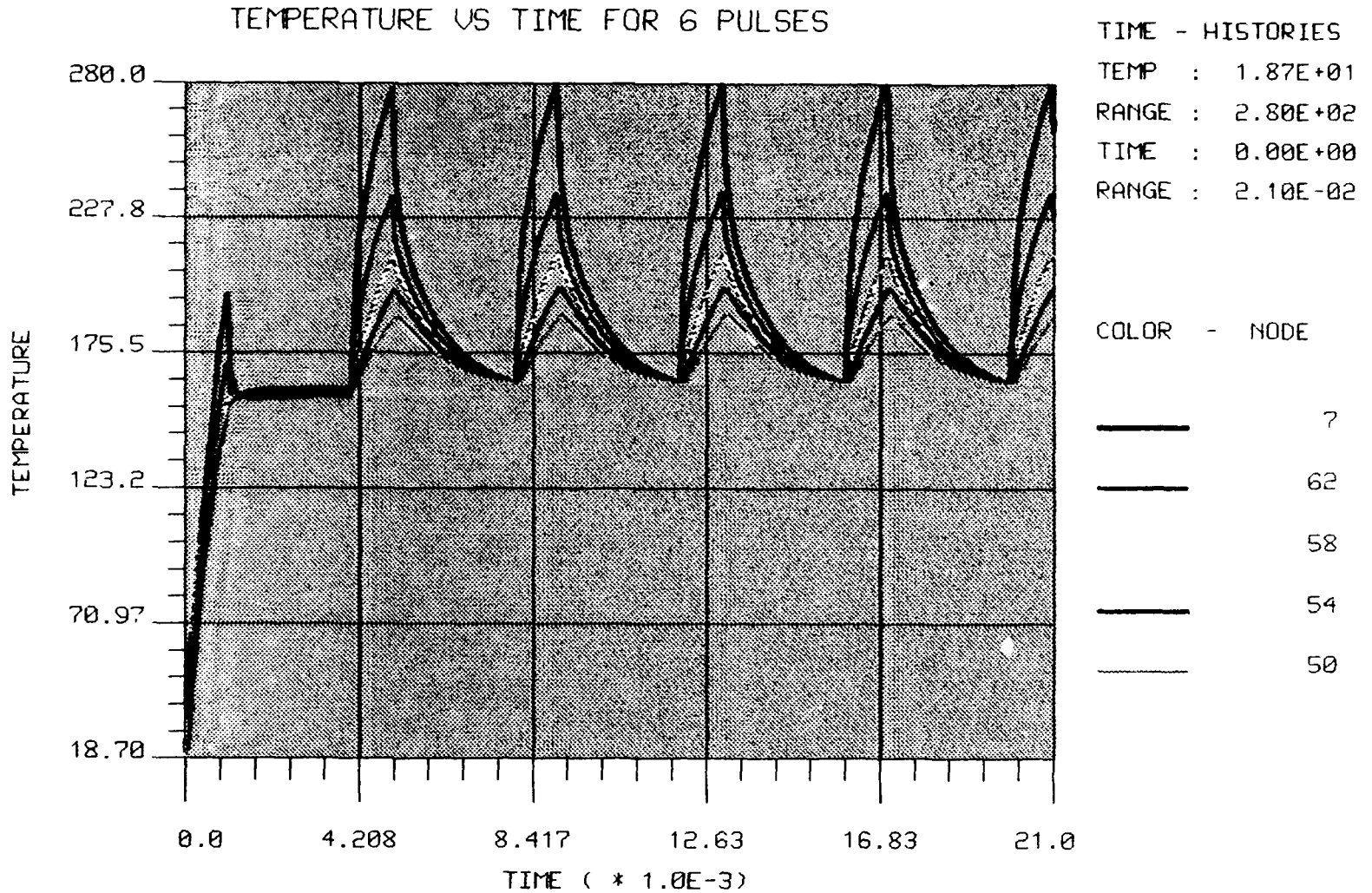
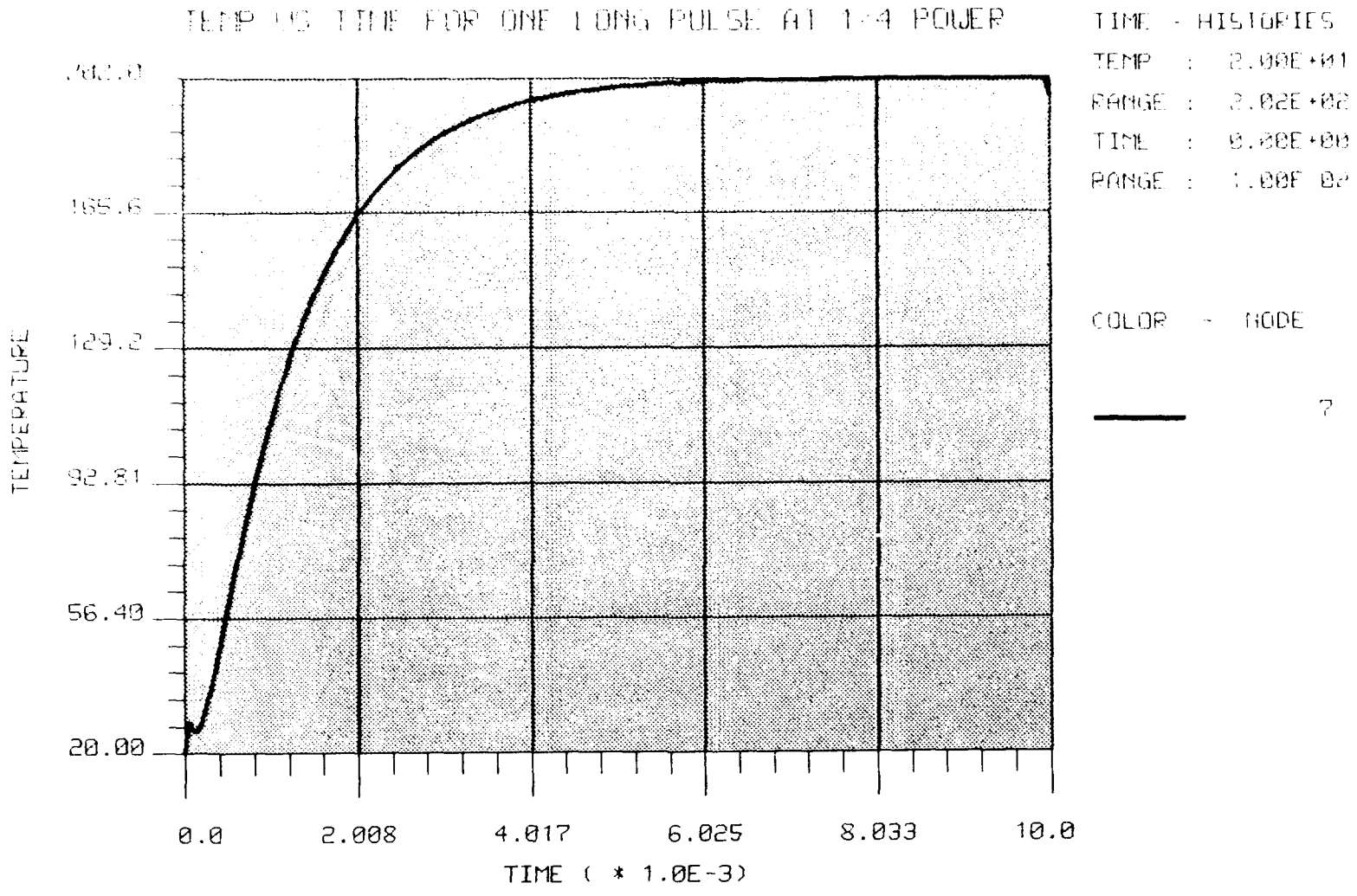


FIGURE 26: TRANSIENT RESULTS USING IMPROPER TIME STEP



2-D TRANSIENT HEAT TRANSFER/QUARTER MODEL

FIGURE 27: TRANSIENT RESULTS FOR SIX PULSES



2-D TRANSIENT HEAT TRANSFER/QUARTER MODEL

FIGURE 28: TRANSIENT RESULTS FOR ONE LONG PULSE

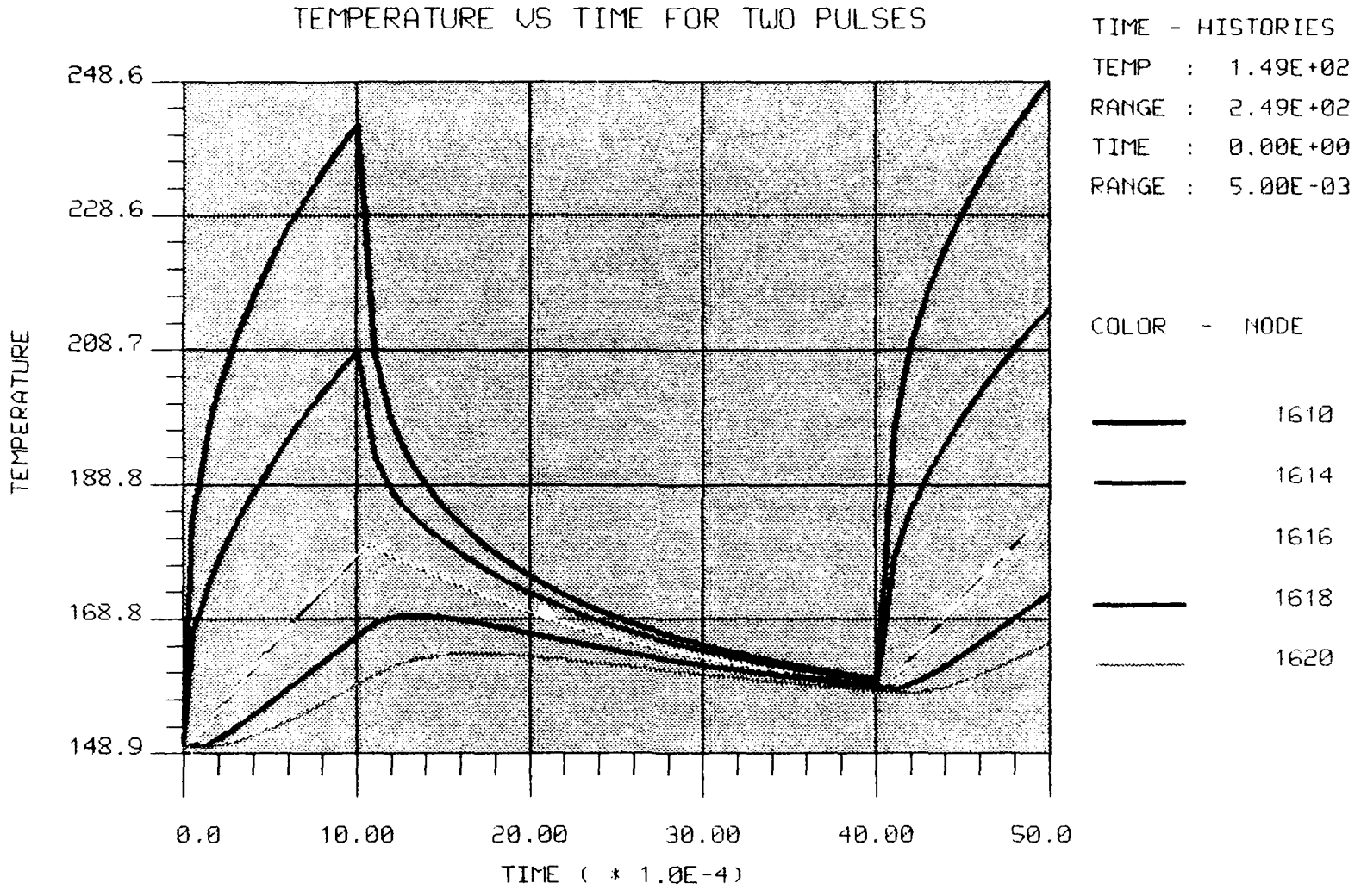


FIGURE 29: 3-D MODEL TRANSIENT RESULTS, NODES 1610-1620

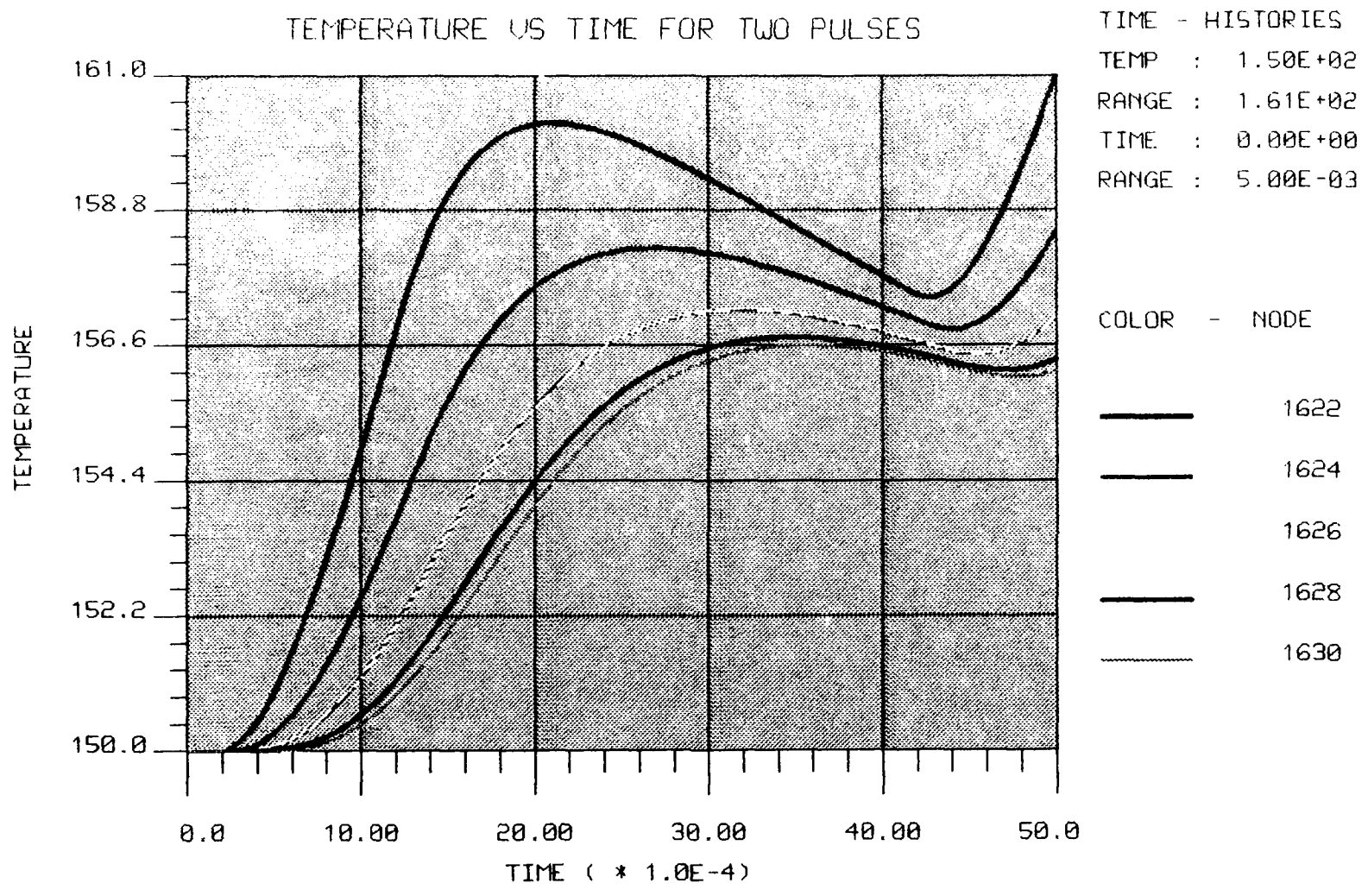


FIGURE 30: 3-D MODEL TRANSIENT RESULTS, NODES 1622-1630

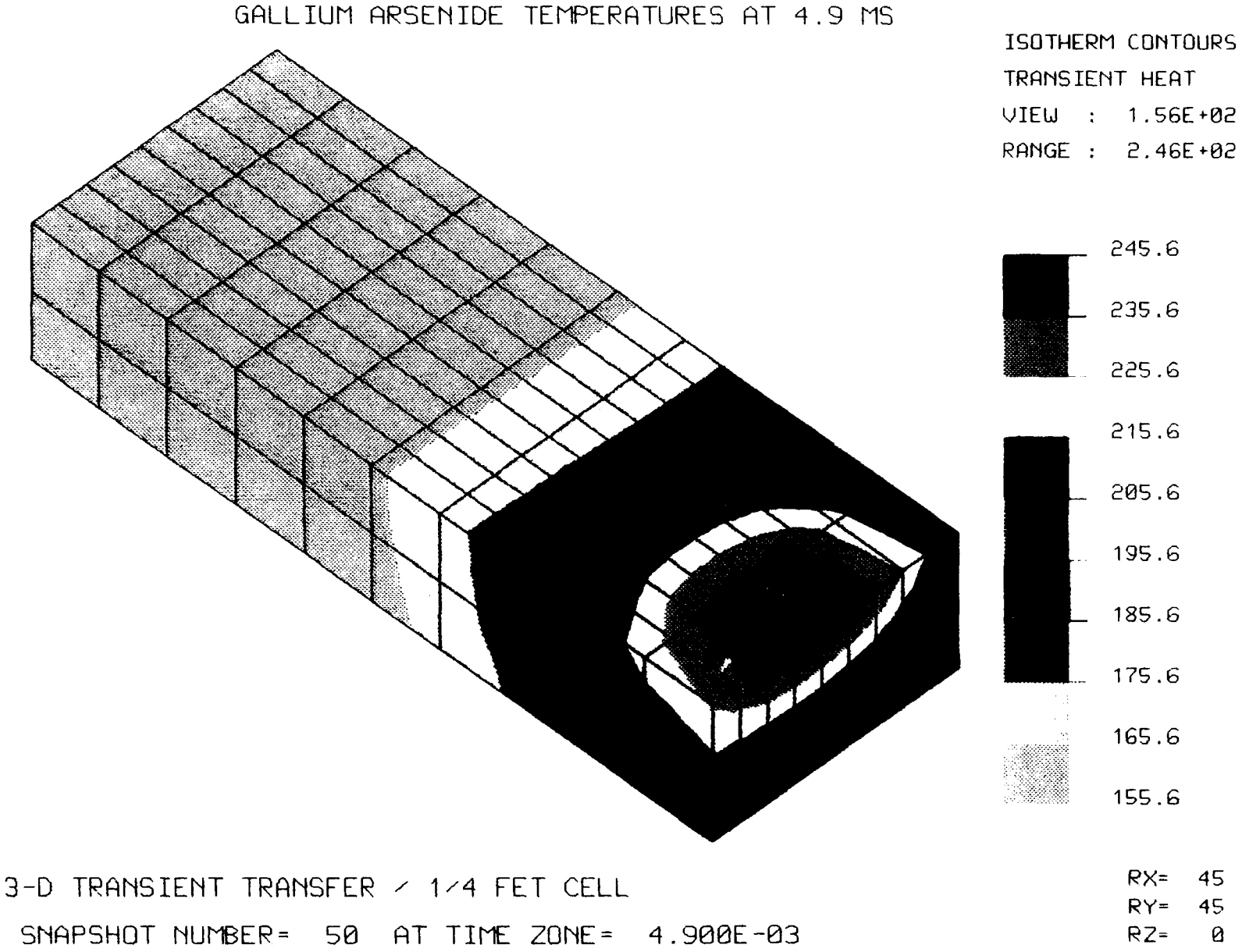


FIGURE 31: GALLIUM ARSENIDE MAXIMUM TEMPERATURES

Figures 29 and 30 are:

NODE	DISTANCE FROM CENTER OF CELL (Micrometers)
1610	0
1614	100
1616	150
1618	200
1620	250
1622	300
1624	350
1626	400
1628	450
1630	500

Figure 31 shows the temperature contours for only the gallium arsenide at a time of 4.9×10^{-3} ms, just before the end of the second pulse. These temperatures are peak values, and comparison with the steady state results shown in Figure 6 show the active region of the chip (the first two rows of elements in the Z-direction) to have peak values 55 degrees higher than steady state results.

As the distance from the active region increases, the peak values approach the steady state values. For example, midway along the length of the model (250 micrometers from the center of a cell), the peak temperature is approximately 165 degrees and the steady state value is also approximately 165 degrees. Figure 29 showing the response of node 1620 at Z = 250 micrometers indicates the small fluctuation of temperature with time. Node 1620 is 150 micrometers beyond the end of the gate.

5.0 CORRELATION OF FINITE ELEMENT (F.E.) AND INFRARED (IR) TEMPERATURES

The RADC Reliability Testing Program for microwave/millimeter wave devices will include temperature measurements using a Barnes Computherm Infrared Imaging System. It is expected that the IR measurements and the F.E. results will differ. The IR device measures temperatures over a region no smaller than 15 micrometers which is much larger than the 2 micrometer region where the heat is generated. Also, it cannot follow the rapid temperature change during a pulsed operation. The F.E. results, on the other hand, depend on the accuracy of the physical and material properties used for the simulation. However, the combination of data can make better assessments of maximum temperatures possible. Consider first the variation of temperature over distance. Figures 15 and 17 show localized views of the temperature distribution under steady state conditions. Figure 15 is a worse case situation with heat applied in a 1 micrometer wide region. In order to compare these results to an IR measurement, the F.E. results must be averaged similarly to the averaging done by the IR Imaging System. The procedure proposed would be to integrate the absolute temperature raised to the fourth power over the area of the IR sensor, and then compute the average temperature by dividing this result by the sensor area. For this application, Figure 15 indicates one could ignore the variation of temperature in the Z-direction and integrate only over the X-direction. Figure 32 is a plot of absolute temperature to the fourth power vs. location, based on the F.E. results of Figure 15 for a 15 micrometer spot centered over the gate. Graphically integrating the area under the curve from absolute zero to the temperature indicated and over the 15 micrometer spot-size dimension results in a value of 6.9176×10^{11} $(°K)^4 \mu M$.

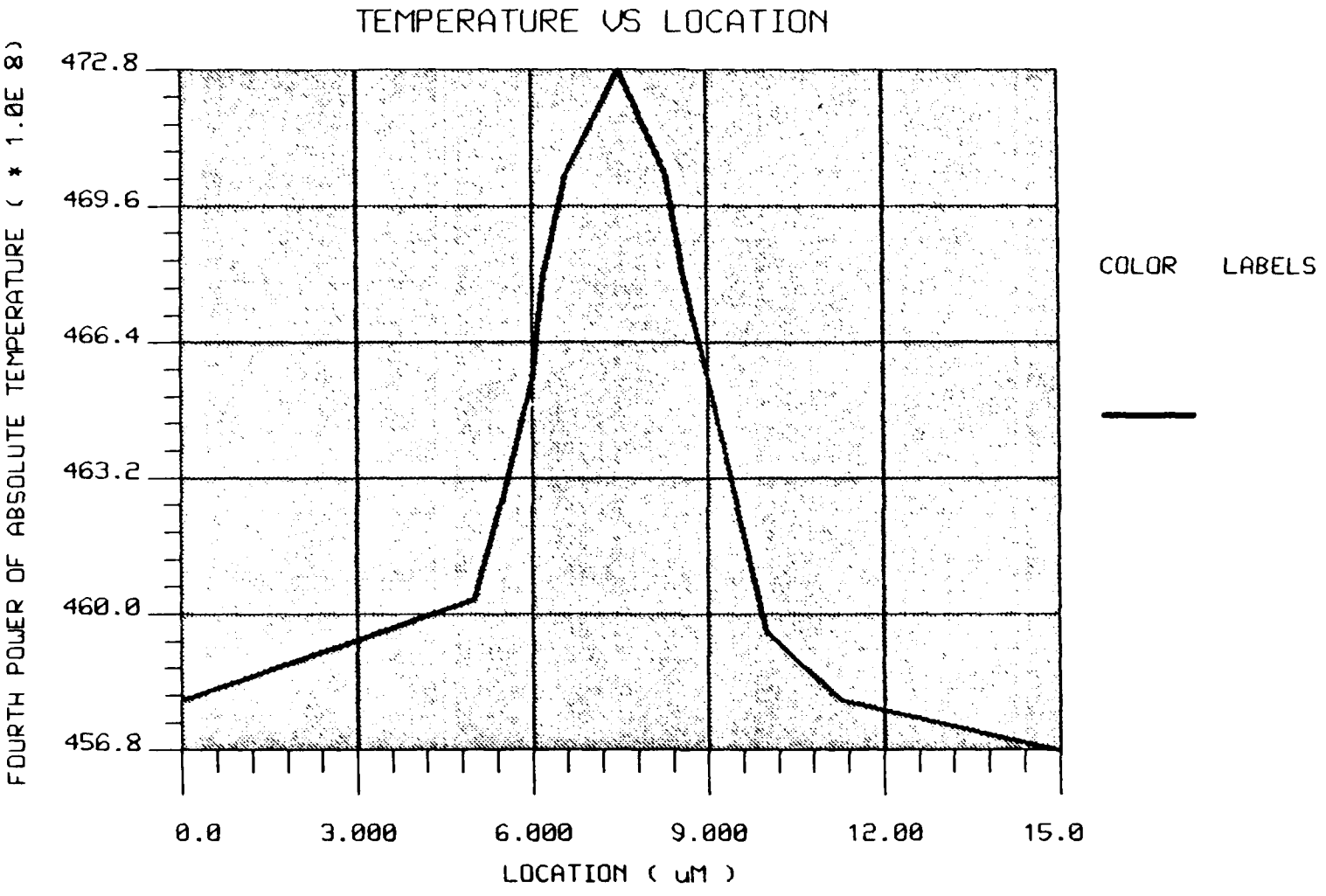


FIGURE 32: FOURTH POWER OF ABSOLUTE TEMPERATURE OVER IR SENSOR REGION

Dividing by the spot-size dimension of 15 micrometers gives an average value of 4.6117×10^{10} $(°K)^4$. Taking the fourth root and subtracting 273 results in an average temperature of 190.4 degrees. Although time consuming, this procedure allows an equivalent finite element average temperature that can be compared to an infrared measurement.

Should the F.E. equivalent average temperature differ significantly from the IR measured value, one could either modify one or more of the values used for thermal conductivity or modify the magnitude of heat generated in the model. Because the temperature increase is related to both the overall thermal resistance and the heat dissipated, either modification would be acceptable. However, the distribution of temperatures is primarily affected by the thermal conductivity of the chip material.

This effort has shown that the 3-D model of one quarter of a FET cell produces maximum temperature results nearly identical to the results produced by the single gate model. Furthermore, the single gate model doesn't show a large temperature gradient over the 15 micrometer spot size of the IR sensor. For this particular amplifier chip, if a significant difference occurs between the F.E. results from the one-quarter FET cell model and the IR measurements, then the quarter model will be adjusted by varying the value for gallium arsenide thermal conductivity. The IR measurement should be made under a nonpulsed condition. The adjusted value of gallium arsenide thermal conductivity will then be used to perform the transient simulation. Because the IR sensor cannot follow the pulsed response of the transistors, the maximum temperature obtained from the transient F.E. analysis should be used as the best estimate of the highest temperature within the transistor circuit.

6.0 SUMMARY AND CONCLUSIONS

The purpose of this effort is to determine the means to acquire knowledge about the temperatures within Microwave/Millimeter Wave Monolithic Integrated Circuits (MIMIC). Various MIMIC devices will be life tested at RADC, and knowledge of the maximum operating temperatures is essential in order to thoroughly assess reliability. Finite element thermal simulations make possible a prediction of the temperatures due to heat dissipations in the extremely small regions of an integrated circuit and also under conditions where temperatures change very rapidly with time. Several 3-dimensional and 2-dimensional models of a C-band module driver amplifier chip were developed and both steady state and transient simulations were performed. The objectives accomplished are:

1. Determination of the temperature increase between the module base and the gate region of the FET cells
2. Identification of the proper finite element modeling procedures and techniques
3. Estimation of the thermal effects of IC metallization
4. Investigation of various methods of simulating heat generation
5. Investigation of correlating infrared thermal measurements with finite element analytical results.

Three 3-dimensional models were developed. The models are one half of a six transistor chip, one quarter of one transistor cell, and a single gate region of a transistor cell. The chip model showed several adiabatic lines of zero heat flow that determine the boundaries for follow on finite element models of smaller regions of the chip. The chip model also showed

significant heat flow in all three dimensions. The one quarter of one transistor cell model proved to be very adequate for obtaining the temperature increase between the module base and the maximum temperature of the cell. Under steady state conditions using an average heat dissipation of 2.31 watts per chip, the increase in temperature was approximately 90 degrees. This model also showed that generating heat as a flux loading over the active region of the GaAs produced results nearly identical as generating heat at the node points along the lines where the source and drain elements are connected. The model of a single gate region of a transistor cell showed maximum temperatures nearly identical to the quarter cell model. The single gate model, however, is able to provide better detail of the temperature distribution in and around the gate region. This model, as well as the quarter model, showed an approximately 5% reduction in temperature rise due to source metallization extending through the via in the chip. For practical purposes, the source and drain metal can be neglected in finite element thermal simulations. The single gate model showed a low sensitivity to the method of heat generation, and it appears unnecessary to model heat generation with cylindrical shaped elements.

Several 2-dimensional models were developed, simulations performed, and results compared with the 3-dimensional simulations. If a 2-dimensional simulation is performed, it is best to use a plane along the gate "width" direction and to ignore the heat flow along the gate "length" direction. The best 2-dimensional model produced results 13% higher than the 3-D results. The accuracy of a 2-D simulation depends on the spacing of the transistor cells on the chip. In general, if computer resources are available, 3-D simulations should be performed.

Transient simulations are essential if the device operates in a pulsed mode. For this device, it would take approximately 6 ms for steady state conditions to be reached. Therefore, any on/off cycling less than 6 ms would require a transient thermal simulation. The 3-dimensional transient simulation using the one-quarter cell model showed peak values 55 degrees higher than steady state results for a 1 ms on /3 ms off pulse.

The single gate model was useful in showing the temperature distribution in a very localized region of the transistor cell. A procedure is proposed that would allow an averaged finite element temperature to be calculated that would be similar to the averaging done by an IR Imaging System. This would make possible a comparison of finite element results with IR measured results even though the IR sensor averages the temperatures over a relatively large region compared to the heat generation region. If significant differences exist, the F.E. model could be modified either by changing material properties or the value of heat generation. It is suggested the material properties be adjusted. After satisfactory agreement has been achieved between the averaged steady state F.E. simulation results and the IR measured temperature for the device in a nonpulsed mode of operation, the adjusted values of material properties can be used with knowledge of the pulsed operation to perform the transient simulation. The procedure requires integrating the absolute temperature raised to the fourth power over the area of the IR sensor, and then computing the average temperature by dividing this result by the sensor area. Because the IR sensor cannot follow the pulsed response of the transistor, the adjusted transient F.E. analysis should be used for the best estimate of the nighest temperature within the transistor circuit. Finally, for this

device, the transient simulations indicate that temperatures beyond 150 micrometers past the gate remain reasonably constant with time.